Investigation of Topology Candidates for 48V VRM

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Abstract— In future applications, it will be impractical for voltage regulator modules (VRMs) to draw power from the 12V output of the silver box because the voltage bus will be too low to deliver more power. Therefore, distributed power systems (DPSs) with buses of 48V will be more feasible solutions for future high-end PCs. This paper focuses primarily on the investigation and comparison of 48V VRM candidates. Six 48V VRM prototypes are built and compared: the active clamp forward, asymmetrical half bridge, symmetrical half bridge, push-pull, push-pull forward and integrated-filter push-pull forward topologies.

I. INTRODUCTION

In the last decade, the computer industry’s development has been dramatic. The speed and integration density of microprocessors have increased rapidly. The next generation of processors will work in clock frequencies of 2GHz and even 10GHz. As a result, modern microprocessors are being designed to work with lower levels of voltage to meet higher and higher speed and efficiency demands. So the requirements for the microprocessors’ power supplies are more critical. It is impractical to supply power to these microprocessors directly from the 5V output of the silver box. From the Pentium processor, a non-standard power supply of less than 5V is used as a dedicated converter in order to provide high output current at low output voltage. This power supply is known as a voltage regulator module (VRM).

Future VRMs will also encounter the transition problem. During transition from light load to heavy load, the processor may demand a current of from 1A to 130A, at a high slew rate of up to 150A/us[16]. However, the transient voltage tolerance will be much smaller. Fig. 1 shows the Intel CPU voltage and current road map.

Most of today’s VRMs draw power from the 12V output of the silver box. However, this 12V voltage bus will be too low to be feasible for future low-voltage, high-current applications especially the high-end workstation and server applications. As an alternative, distributed power systems (DPSs) with voltage buses of 48V, may be more practical for future computer systems, such as servers and high-end workstations. Compared to the low-voltage bus DPS, the high voltage bus DPS is easy to use. The conduction loss of the high-voltage bus DPS is lower and the distributed bus is easy to design. In a high-voltage DPS the transient response of the load has less effect on the bus voltage, and then less effect on the other loads. The input filter size of the high voltage input VRMs can be reduced significantly[1]. Another merit of 48V-input VRMs is that because transformers are used, the duty cycle can be optimized for efficiency, ripple canceling effect and transient by adjusting the turns ratio. This paper focuses primarily on the comparison of several 48V VRM topology candidates.

II. PRIMARY AND SECONDARY SIDE TOPOLOGY SELECTION

When 48V bus voltage is used, isolation is required not only for safety consideration but also for design optimization. For the isolated low output voltage topologies, secondary-side conduction loss is dominant and is the major factor in the converter's level of efficiency. So the current doubler with integrated magnetics (IM) is preferred for two reasons[4,5]. First, it reduces the rms value of the output inductor current and transformer secondary side current. The total conduction loss of the output inductor and transformer secondary side windings is reduced significantly. Second, the current doubler reduces the output voltage ripple by canceling the current of two output inductors. As a result, the required output filter size is decreased. This is important for VRM applications because of the very high power density and transient response requirements. Furthermore, by using integrated magnetics, the number of high-current interconnections is minimized and the transformer and inductors can be integrated on a single core to simplify the package and layout[6,7]. As a result, the overall size and volume is minimized and higher power density can be achieved.

Generally, the current doubler topology can be used with almost all symmetrical primary-side topologies, such as symmetrical half-bridge, push-pull, full-bridge, etc., for low-voltage, high-current applications. Fig. 2 shows the current doubler rectifier and it’s operating waveforms when it is symmetrically controlled. If the primary side is not...
symmetrically controlled, there is no off-time interval during which the two switches' currents will share the total current. In that case, the rectification loss is not minimized\[5\]. Fig. 3 shows the normalized synchronous rectifier rms current of symmetrical and asymmetrical half bridge with current doubler. The calculation is based on the assumption that the output current ripple is 10% of the output current \(I_o\) and the results are normalized by output current \(I_o\). Fig. 4 shows the normalized inductor rms current. The normalized transformer secondary side rms current is shown in Fig. 5. From Fig. 3 we can see that for symmetrically controlled current doubler the smaller the duty cycle, the smaller the rms current of the synchronous rectifier. But small duty cycle need large inductance and will increase primary side current which will cause large conduction loss and switching loss. The optimum duty cycle design is a trade-off between primary and secondary side loss as well as input voltage range.

From the above point of view, the forward-flyback, asymmetrical half bridge and 50% duty cycle half bridge or full bridge are not good for low voltage high current applications. For phase shift ZVS full bridge, the freewheeling current in the primary side of the transformer will reflect to the secondary side. So even the synchronous rectifier is turned on, the current through it is the difference between the inductor current and secondary side winding current that is reflected from the primary side winding freewheeling current. As a result, the current waveform of the synchronous rectifier is changed as shown in Fig. 6. The rms current in secondary side synchronous rectifiers will increase. So only symmetrical half bridge, push-pull, hard switching full bridge and phase shift ZVZCS full bridge are suitable here. The phase shift ZVZCS full-bridge topology may be the best choice at high frequency, but it is not considered here because of it’s higher component count. Hard switching full bridge is not preferred not only because the higher component count but also higher switching loss, conduction loss and gate driving loss. When switching frequency is high, the switching loss will be comparable to secondary-side conduction loss. Then the conclusion will be different.

![Figure 1: Intel CPU voltage and current road map.](image1)

![Figure 2: Current doubler rectifier and its operating waveforms.](image2)

![Figure 3: Normalized synchronous rectifier rms current.](image3)
Fig. 4. Normalized inductor rms current.

Fig. 5. Normalized transformer secondary side rms current.

Fig. 6. Operating waveforms of phase shift ZVS full bridge with current doubler.

III. 48V-INPUT TOPOLOGY CANDIDATES FOR VRM

A. Active Clamp Forward (Forward-Flyback) VRM

Fig. 7 shows the active clamp forward VRM. The secondary side synchronous rectifier conduction loss is large as mentioned before. The detailed analysis of this circuit can be found in [4]. The advantage of this circuit is low turn-on loss due to ZVS turn-on of the primary side main-switch. The disadvantage is that the transformer has a significantly lower magnetizing inductance in order to generate the dc magnetizing current needed to support the secondary side current during off time [4]. This will cause large conduction loss and turn-off loss as well as transformer core loss.

B. Asymmetrical Half Bridge VRM

Fig. 8 shows the asymmetrical half bridge VRM. As mentioned before, the secondary side conduction loss of synchronous rectifier is large. The advantage of this circuit is low turn-on loss due to ZVS turn-on of the primary side switches. The disadvantage is that it’s a fourth-order system, control design is complicated. And the current in two inductors are different, so the integrated magnetics design is also complicated.

C. Symmetrical Half Bridge VRM

Fig. 9 shows the symmetrical half bridge VRM. One merit of the half-bridge topology is that when the primary side switch turns off, the voltage of the switch is clamped to the input voltage. But the primary side winding current will double because only half of the input voltage is applied to the primary side winding. Although lower voltage rating switches can be used and a smaller snubber is needed, the primary side switch conduction loss and switching loss are large.

D. Push-pull VRM

Fig. 10 shows the push-pull VRM. The push-pull converter’s efficiency is limited by the leakage inductance. When the primary side switch turns off, the leakage inductance of the transformer induces a large voltage spike, which means large switch turn-off loss. The spike also means that switches with higher voltage ratings are needed. The higher the voltage rating, the larger the drain source Rdson of the MOSFET, and the larger the conduction loss. Although snubbers can be used, lossless snubbers will increase the complexity of the circuit, and large nonlossless snubbers will impair efficiency. Due to the leakage inductance bottle-neck, the push-pull VRM can not be expected to have high efficiency.

E. Push-pull Forward VRM

There are various solutions to the leakage inductance problem. One is the push-pull forward VRM, which employs a clamping capacitor to solve the spike issue [3, 12]. Fig. 11 shows the topology and it’s operating waveforms. With the clamping capacitor, the voltage on the primary side switch will be limited to twice the level of input voltage. In the meantime, the current of the primary side switch is kept the same, which means the switching loss of the primary side MOSFET can be reduced. Furthermore, lower voltage rating devices can be used to decrease the conduction loss. Moreover, unlike the push-pull topology, the winding current is shared between two primary side windings. As a result of the reduction in the rms value of the primary side
winding current, the conduction loss of the primary side winding is also reduced. Fig. 12 shows the normalized (by \(I_oV_o/V_{in}\)) rms current value of the primary side winding in the push-pull and push-pull forward topologies.

Another benefit of the push-pull forward topology is that the input current is continuous. This reduces both the rms value of the input current and the conduction loss. Fig. 13 shows the normalized (by \(I_oV_o/V_{in}\)) rms current value of the input current in the push-pull and push-pull forward topologies. Furthermore, the input filter size can also be reduced.

**F. Integrated-filter push-pull forward VRM**

Recently, the integrated-filter push-pull forward topology was proposed[8]. Shown in Fig. 14, this topology requires an additional clamping capacitor and more primary side windings. If integrated magnetics design is used no additional windings are needed[8]. The only requirement is that the windings be split and the windings and switches be rearranged. The switch and winding current of the improved push-pull forward topology are the same as the original one, but the input current is almost flat because two windings conduct the input current and the ripples cancel each other. Therefore the input filter is a built-in function of this new topology, and the leakage inductances of the primary side windings are utilized as the input filter[9, 13, 14]. As a result, the input filter conduction loss is minimized and higher efficiency can be expected. Furthermore, the input filter size can also be reduced.

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**Fig. 7. Active clamp forward VRM.**

**Fig. 8. Asymmetrical half bridge VRM.**

**Fig. 9. Symmetrical half bridge VRM.**

**Fig. 10. Push-pull VRM.**

**Fig. 11. Push-pull forward VRM.**
Fig. 12. Normalized transformer primary side winding rms current.

Fig. 13. Normalized input rms current.

Fig. 14. Integrated-filter push-pull forward VRM.

IV. EXPERIMENTAL RESULTS

For experimental evaluation, several 48V VRM prototypes were built. First, the active clamp forward with current doubler was built. The primary side device are IRF3415(150V, 42mΩ, Qg = 200nC) for S1 and IRF630(200V, 0.3mΩ, Qg = 35nC) for S2. For each synchronous rectifier 2 SUP75N03-04(30V, 4mΩ, Qg = 200nC) are paralleled. The integrated magnetics is used on a Philips E32-3F3 core. The 14-turn primary side winding is built on a multi-layer 6-oz PCB and the 1-turn secondary side winding is copper foil. The 100kHz 48V/1.2V 70A prototype efficiency is shown in Fig. 15.

Fig. 16 shows the efficiency comparison push-pull forward, symmetrical and asymmetrical half bridge converters. All the three converters’ input voltages are 48V and their outputs are 3.3V 30A output at 200kHz switching frequency. For the comparison among the VRMs, the same secondary side circuits are used. For each synchronous rectifier 2 MTP75N03HDL(25V, 9mΩ, Qg = 122nC) are paralleled. The only difference is the primary side circuit and transformer turns ratio. For both the symmetrical and asymmetrical half bridge, the transformer turns ratio is 3 to 1 and switches are IRF540(100V, 44mΩ, Qg = 71nC). For push-pull forward, the transformer turns ratio is 6 to 1 and switches are IRF3315(150V, 70mΩ, Qg = 95nC). At full load, the efficiency of push-pull forward converter is 2~3% higher than that of half bridges.

Finally, the symmetrical half bridge, push-pull, push-pull forward and integrated-filter push-pull forward converters are compared under 48V input, 1.2V 70A output at 100kHz switching frequency. To both minimize the secondary side conduction loss and simplify the layout, one turn is used in the secondary side winding. To reduce the equivalent resistance, skin effect, leakage inductance and proximity effect, a multi-layer interleaved PCB winding structure is selected.

The prototypes were built using the following components.

- S1, S2 – PSMN035-150B(150V, 35mΩ, Qg = 79nC), for half bridge is PSMN015-100B(100V, 15mΩ, Qg = 109nC).
- SR1, SR2 – STV160NF02L(20V, 2.5mΩ, Qg = 120nC).
- T, L1, L2 – E32-3F3 Philips E/PLT core, air gap 8mil; multi-layer PCB windings; primary side: 8 turns of 2-oz(70µm) PCB copper, for half bridge is 4 turns; secondary side: 1 turn of 2-oz(70µm) PCB copper; L1 = L2 = 360nH; leakage inductance measured on the secondary side winding is 10nH. Fig. 17 shows the IM structure.
- Co – 10 x 820 µF, 4V OSCON capacitors plus 20 x 22 µF, 6V ceramic capacitors.
- Cs, Cs1, Cs2 – For push-pull forward Cs = 4 x 3.3 µF, 100V ceramic capacitors; for improved push-pull forward Cs1 = Cs2 = 2 x 3.3 µF, 100V ceramic capacitors.

Fig. 18 shows the prototype of the integrated-filter push-pull forward VRM. Figs. 19 - 22 show the experimental waveforms of the four VRMs. As these figures illustrate, the integrated-filter push-pull forward and push-pull forward topologies have the same primary side winding current, which is smaller than that of the push-pull topology; the push-pull forward topology has a smaller input current than the push-pull topology and the integrated-filter push-pull forward topology has almost flat input current. The experimental results closely match the analysis.

The four VRMs’ efficiencies are measured, as shown in Fig. 23. As can be seen, the integrated-filter push-pull...
forward VRM has the highest efficiency in heavy load range. The efficiencies peak in the 20A-25A load range. At higher loads, efficiency decreases rapidly due to the increase of the conduction loss that occurs with the current increase.

Fig. 15. Efficiency of active clamp forward.

Fig. 16. Efficiency comparison.

Fig. 17. Integrated magnetics structure.

Fig. 18. Prototype of the integrated-filter push-pull forward VRM.

Fig. 19. Experimental waveforms of symmetrical half bridge.

Fig. 20. Experimental waveforms of push-pull.

Fig. 21. Experimental waveforms of push-pull forward.
V. CONCLUSION

There are many topologies that can be used for the 48V-input VRM such as active clamp forward, asymmetrical half bridge, symmetrical half bridge, push-pull, push-pull forward and integrated-filter push-pull forward. The different primary and secondary side topologies are discussed and compared. For high current low voltage applications, the current doubler with integrated magnetics is preferred to reduce the conduction loss. Six converter prototypes were built and compared. The integrated-filter push-pull forward topology has high efficiency which makes it a very promising candidate for the 48V VRM.

REFERENCE
