Design of Power MMICs and Power Combining Techniques

Inder J. Bahl
ITT Gallium Arsenide Technology Center
7670 Enon Drive
Roanoke, VA 24019
USA

Abstract
The current trends in power transmitters for advanced military microwave systems are demanding increased integration, reliability, radiation hardness and lower cost when produced in large volume, whereas the microwave commercial market mandates low cost. The Monolithic Microwave Integrated Circuit (MMIC) technology for power amplifiers promises to meet these requirements and provides microwave designers a high volume manufacturing process. In this paper the design considerations for narrow band, broadband and multistage power MMICs are discussed. Examples of power MMICs developed using MSAG FET technology for narrow band and broadband applications are described. Power combining on the chip as well as using a hybrid MIC approach are discussed.
1. Introduction

In comparison to power tubes, microwave power MESFET amplifiers are compact in size, lightweight, low cost, more reproducible, more efficient and reliable, and they operate at lower supply voltages. These amplifiers require much shorter warm-up time and no adjustment in the bias as well as in the circuit is required over long periods of operation. The performance of MESFET amplifiers is constantly improving in terms of output power, power-added efficiency, linearity and frequency. Although individual GaAs FETs do not provide power levels comparable to bipolar and TWT amplifiers, their use in conjunction with efficient power combining techniques appears to offer a viable solution. Power monolithic microwave integrated circuit (MMIC) amplifiers using MESFET technology look attractive for realizing tens of watts of power; these chips can be combined further using standard hybrid MIC techniques to obtain much higher power levels [1-12]. High-efficiency operation of these circuits is becoming one of the most important factors for reducing prime power and cooling requirements for advanced microwave and millimeter wave systems. These characteristics are particularly useful for space and military applications where weight, size, and power-added efficiency requirements can impose severe limitations on the choice of components and systems.

MESFET power amplifiers are complementary to Si bipolar transistors in that below 1 GHz, Si bipolar is preferred for high power and high efficiency, while above 1 GHz, GaAs MESFETs achieve the high power, high gain and high efficiency that silicon devices cannot. MESFET power amplifiers have several advantages compared to HBTs in terms of planar technology, good distribution of power dissipation which results in higher reliability, smaller number of steps in fabrication, high frequency and high RF output power operation. When they are compared with HEMT, they are more reliable, have higher power output and are low cost at microwave frequencies.

The current trend in microwave technology is toward circuit miniaturization and integration, improved reliability, radiation hardness, low power consumption, cost effectiveness and high volume consumer electronics. Component size, weight and higher level of integration are prime factors in the design of electronic systems for satellite communications, phased-array radar systems, electronic warfare, and other airborne applications. High volume and low cost are the primary drivers in the consumer electronics market. MMIC technology fulfills the above performance requirements and also has the potential of producing subsystems on a single chip costing less than $100; ICs with single microwave functions can be obtained for less than $3. In addition, a new upsurge in commercial and military millimeter wave applications supported by new devices has created tremendous interest in the monolithic technology where the effect of bond-wire parasitics can be minimized and where subsystem cost can be lowered by a factor of ten or more compared with hybrid solutions.

In fabricating MMICs, all active and passive circuit elements and interconnections are formed together on the surface of semi-insulating substrate (usually gallium arsenide). Typically power MMICs use microstrip and metal-insulator-metal (MIM) capacitors for
the matching networks, whereas at low microwave frequencies lumped inductors and MIM capacitors are commonly used. Typically, power MESFETs are fabricated with a recess gate process, but the self-aligned gate process is gaining popularity because of its ability in processing devices optimized for different functions, such as analog and digital on the same wafer at the same time [13-15]. The ITT multifunction self-aligned gate (MSAG) process being used for MMICs is also superior in terms of manufacturability, reproducible performance, and RF yield.

Over the past decade, power MMICs have been upgraded from laboratory curiosities to qualified production hardware for the commercial and military markets. A major factor in the success of power MMICs has been the advancement in: the materials, processing technology, devices, non-linear models, CAD tools, automated on wafer testing and packaging. The concept of implementing a “system on a chip” having a transmitter on it is now becoming a reality in monolithic microwave technology. Major advantages of power MMICs and MMIC-based high power amplifiers include low cost, small size, low weight, circuit design flexibility, broadband performance, elimination of circuit tweaking, high volume manufacturing capability, package simplification, improved reproducibility, radiation hardness and improved reliability.

During the past decade there has been significant progress in monolithic power amplifiers operating over both narrow-bands and broad-bands. Power levels of 12 watts and 0.75 W/mm power density (output power density per unit gate width of MESFET), from a single MMIC chip at C-band with 36 percent power-added efficiency, and 0.65 W/mm² power density for the chip area (output power density per unit area on GaAs) have been demonstrated. A 6-watt MMIC chip has been developed at X-band [16], whereas, at 30 GHz, 2 watts of power output has been obtained [17]. In the high-efficiency area, a C-band MMIC amplifier with 70% PAE, 8 dB gain, and 1.7-watt power output has been demonstrated [16]. For broadband amplifiers having an octave or more bandwidth, MMIC technology is very promising and has been exclusively used. Figure 1 depicts current status for MMIC amplifiers working up to millimeter wave frequencies. FETs used in the millimeter frequency area are sub-half micron gate length. State-of-the-art in high efficiency and broadband power MMICs is summarized in Table 1 and 2, respectively. The high efficiency examples included in Table 1 have at least a 40% PAE.

This paper provides an overview of power MMICs and design considerations for narrow-band, broadband, multistage and high efficiency power amplifiers. Design techniques for efficient power combining on the chip as well as using hybrid MIC approach are discussed.

2.0 MMIC Power Amplifier Design

The design of power amplifiers includes the selection of FET periphery, source and loadpull data or device model, synthesis of matching networks, biasing networks (including bias voltage, current budget, and realization of amplifiers’ circuitry),
simulation of amplifier performance, on chip power combining, off-chip power combining for higher power level if required, and thermal design. The amplifier design could be narrow band, broadband, or multistage. This section briefly reviews the electrical power amplifier designs and their possible realizations.

A typical design flow diagram for MMIC power amplifier is shown in Fig. 2. The performance requirements in terms of frequency band, gain, power out, PAE, input and output VSWR, etc. determine the FET sizes, the circuit design topology including matching, the number of stages, the aspect ratio for the FETs between the stages, and the substrate thickness. In order to minimize the size effects on performance degradation in combining power at higher frequencies, a properly selected unit cell (optimized in terms of unit gate width and gate-to-gate pitch) must be used and fully characterized. In power amplifier design a proper aspect ratio plays a very important role in realizing a high PAE amplifier. For MMIC power amplifiers, the GaAs substrate thickness is usually 75 to 100 µm (3 to 4 mil). Thinner substrates have lower thermal resistance, while the thicker substrates provide lower circuit losses and are easier to handle.

The selection of circuit topology depends upon the bandwidth. The matching networks are generally designed to provide the required bandwidth with suitable guard bands; the matching elements have small size, they are easy to manufacture and they have high yield. In order to reduce size, biasing circuitry is generally a part of the matching network. The drain voltage is directly connected to the top of the RF bypass capacitor (low impedance point) and the gate bias is brought to the device through a suitably selected resistor which also provides isolation between the device and the power supply. In this biasing scheme no quarter-wave or choke is required, thus reducing chip size. Generally, MIM capacitor values of 20 and 10 pF are adequate at C-band and X-band. The design of high PAE amplifier MMICs require special care for reactive harmonic termination, whereas the low frequency (0.4 to 3 GHz) applications mandate compact size and low cost. High PAE designs require extreme care in output impedance matching at the fundamental, 2nd and 3rd harmonic frequencies. High PAE low-frequency designs also require very low loss inductors at the output and offchip chokes for biasing. Low-pass matching networks provide good rejection for high frequency spurious and harmonic frequencies but have a tendency to ward high gain at very low frequencies. Both even- and odd-mode stability [20] analysis must be performed to ensure the circuits are stable; if required, proper stabilization circuits must be used as a part of the matching network.

There are several methods which can be used to accurately determine a device's input and output impedance at large-signal conditions, an essential requirement for successful circuit design. The classical load-pull techniques [21-23], large-signal S-parameter data, Cripps technique [24, 25], equivalent circuit [26, 27] and physics-based model [28, 29] are currently being used to determine device input and output impedances. The nonlinear equivalent circuit and physics-based models when used with nonlinear CAD tools, can be used to design power amplifiers and accurately simulate their performance. For narrow band applications, source and loadpull data is
sufficient to design amplifiers. However, for octave or higher bandwidths and very high efficiency applications, nonlinear FET models are essential. To realize successful designs, including multistage amplifiers and predictions of the amplifier's performance in terms of $P_{1\text{dB}}$, PAE, gain, second and third harmonic levels, and third order intercept point, accurate nonlinear models are required.

2.1 Narrow-band Amplifiers

The narrow-band single-stage design consists of first synthesizing input and output matching networks to match source impedance to the input of the FET for maximum gain and, then matching the output of the device to the load for maximum power or high efficiency (or both, depending on the application at hand). As the FET gate width increases to achieve higher power levels, input and output impedances decrease. The input impedance is the most difficult to match. Generally, a combination of lumped and distributed elements is used in realizing impedance matching networks. The output matching network which is designed to deliver maximum power should also be low loss to achieve maximum possible efficiency. Since power amplifiers are usually designed to operate at about the 1 dB gain compression point for maximum output power and PAE, the matching networks are designed to meet small signal and large signal conditions.

As an example, a narrowband MMIC amplifier on a single chip has achieved 10 W power output at 5.5 GHz with an associated gain of 5 dB and a PAE of 36% [30]. Two single-ended amplifiers with outputs combined on a single chip were used to achieve the high power output. Each of the single-ended amplifiers used a pair of reactively-combined FETs with a net 8 mm of FET gate width. Each 8 mm FET is matched to 100 $\Omega$ input and output under maximum power output condition using a linear FET model [30]. Both distributed and lumped elements were used in the matching networks. The elements of the output matching network were selected for minimum possible loss with a good match as well as to satisfy electromigration requirements (maximum allowed current density in the bias line was $2\times10^5$ A/cm$^2$). Figure 3 shows the photograph of the amplifier and typical measured characteristics at 5.5 GHz are plotted in Fig. 4. The amplifier has about 6 dB gain and 9 W power output at 1 dB gain compression point.

2.2 Broadband Amplifiers

Broadband amplifier design is carried out by considering the power gain rolloff of the FET with frequency (usually 6 dB/octave), the gain-bandwidth limitations of the input and output of the FET, and the overall amplifier stability versus frequency. The design of a broadband, common-source amplifier requires a compromise between several competing requirements such as bandwidth, power output, gain and power-added efficiency. For such applications, the loadpull technique for FET characterization is not adequate, nonlinear FET models with suitable CAD tools are essential.
There are various techniques used to realize broadband amplifiers including reactive and resistive matching, balanced configuration, series resistive feedback and distributed approach as shown in Fig. 5. Salient features of these amplifiers are summarized in Table 3. The distributed power amplifier has excellent gain-bandwidth characteristics with flat gain and low VSWR, and has the capability of multi-octave bandwidth; however, with limited power output and poor PAE.

Today, high power and moderate to octave bandwidth amplifiers use the balanced configuration which employs two identical single-ended reflective or reactive matching designs combined using Lange couplers. Generally, for high efficiency applications the ICs are combined using the hybrid MIC approach because Lange couplers are more easily realized on thick ceramic substrates than on thin GaAs substrates; also, losses are lower ceramic substrates. This topology can accommodate large reflections from the input and output of the amplifiers and can be easily cascaded for high gain applications. In a single-ended design, when the impedance transformation ratio is larger, it requires more matching elements to realize wider bandwidths. Figure 6 shows the fractional bandwidth as a function of the impedance transformation ratio for VSWR lower than 1.2. If a real load impedance of 10 ohms is to be matched to 50 ohm, over 50% bandwidth, the matching network requires two sections of L-C networks.

An X-band balanced monolithic power amplifier has achieved 2.4 W power output and 26% PAE across the 40 percent bandwidth [31]. Table 2 shows state-of-the-art results for broadband power amplifiers. A distributed amplifier with series capacitors in the gate line to obtain higher power bandwidth product has been reported [32]. This configuration accepts the increased gate width of each FET with increased output power and efficiency. A monolithic GaAs distributed amplifier using 6 x 300 μm FETs has achieved an output power of 0.5 W over the 2 to 21 GHz frequency range with at least 4 dB gain and 14% PAE [33].

A broadband single-stage MMIC amplifier developed using the MSAG FET technology has demonstrated over 3W power output, PAE better than 24% and gain greater than 4 dB over the 10 to 17 GHz frequency range. Figure 7 shows the physical layout of the amplifier and Figure 8 shows the measured performance for three ICs tested from a wafer.

2.3 Multi-stage Amplifiers

The design of a multi-stage power amplifier basically consists of synthesis, analysis and optimization of three matching networks: input, interstage and output. The design of input and output matching networks is similar to the single-stage amplifier design. The interstage matching network usually provides the gain shaping required to compensate for the 6 dB/octave gain roll-off of each FET and also provides enough output power to the succeeding stage for achieving maximum output power from the last stage. The design of the intermediate stage is very critical at high frequencies and for broadband amplifiers. At higher frequencies where gain is lower, the matching must provide
maximum gain as well as power to drive the gate of the next stage for maximum power output. Unfortunately, small signal simulators only do a good job in terms of input match and gain; for high power nonlinear simulators are required to design for high efficiency and wider bandwidths. Interactions between the input and the interstage, and the interstage and the output degrade the power out and PAE over the designed bandwidth if they are not taken into consideration. These interactions might also result in instability in the circuit. Accurate non-linear models and EM simulators play a very important role in the design of such amplifiers.

A broadband two-stage amplifier developed using the MSAG FET technology has achieved over 4W power output, PAE better than 32% and gain greater than 9 dB over the 9 to 14.5 GHz frequency range. Figure 9 shows the physical layout of the amplifier; measured performance is shown in Figure 10. Test data for six ICs from a wafer demonstrate the excellent uniformity across the wafer.

3. Power Combining Techniques

Single FETs are low power devices, and the power output decreases rapidly with increasing frequency due to parasitics and the gate-to-drain transit time. Higher power levels are obtained by combining several FETs on a single MMIC chip. Power levels of 20 W at C-band and 10 W at X-band have been demonstrated. In order to obtain these power levels with high PAE, high across-wafer uniformity of saturated drain-source current (I_{DSS}) and cut-off frequency (f_T) is needed to achieve constant phase and gain for each FET cell. When FET cells are combined in phase using reactive techniques on a single chip maximum power and PAE is achieved. The effect of device uniformity in terms of I_{DSS} and V_P across the wafer on a 4 W broadband IC performance is summarized in Table 4. The experiment numbers 1, 2 and 3 have the same average value of I_{DSS} across the wafers. However, experiment #1 has the best standard deviation in I_{DSS} and V_P, i.e., 6 mA/mm and 0.07V, respectively while experiment #3 has the worst, i.e., 26 mA/mm and 0.5V. At 13.5 GHz, the power output and PAE values are 35.9 dBm and 32.6%, and 34.7 dBm and 27.4%, for experiment #1 and #3, respectively.

The combining loss at the IC or module level play a very important role in developing high PAE power amplifiers. The loss in these networks degrades PAE in three ways: output power reduction, reduction in power gain of the circuit, and for a given RF power out, an increase in dc power. There are several off-chip combining techniques [1] being used depending upon the application at hand. These techniques are summarized in reference [1]. For narrow and broad band applications a modified in-phase Wilkinson is frequently used for low loss. This configuration has excellent amplitude and phase balance characteristics to obtain highest possible combining efficiency. On the other hand, the serial/traveling wave combiner is compact, low loss and has broadband characteristics. In the case of severe requirements for good input and output match, the combiners using Lange couplers, traveling wave and N-way planar having 90° differential line lengths are preferred. Since the combining loss depends upon the
divider/combiner loss, Figure 11 illustrates the combining efficiency as a function of divider/combiner loss for various values of circuit gain. This figure suggests that it is more efficient to combine high gain amplifiers.

A broadband 4-way planar combiner was designed and fabricated on a 15 mil thick alumina substrate ($\varepsilon_r = 9.9$). The circuits were tested back-to-back showing a total measured loss of less than 0.5 dB and a return loss better than 15 dB over the 8 to 16 GHz frequency band. Figure 12 shows a configuration for a planar divider/combiner designed for improved return loss. The combiner loss when connected back-to-back was less than 0.6 dB across the 8 to 16 GHz band. Figure 13 shows a photograph of a pair of 4-way traveling wave divider/combiners in a back-to-back configuration mounted in a test fixture constructed to simulate the final package environment. The width of the test cavity is only about 0.5 cm. Measured and simulated insertion loss and return loss of a pair of TWD/Cs in a back-to-back configuration are shown in Figure 14. The measured loss across the 8-14 GHz frequency range was less than 0.6 dB, which corresponds to a loss of about 0.3 dB per combiner. Also, the minimum return loss measured across most of the band was better than 15 dB.

Figure 15 shows the assembly details of the 12 W broadband power amplifier and measured performance is shown in Figure 16. The minimum power and PAE obtained over the 9.2 to 14.1 GHz were 11 W and 23%, respectively.

4. Conclusion

Advances in MMIC power amplifier technology are reviewed. Monolithic IC technology promises to meet the power amplifier requirements of high performance and low cost for active aperture radars, electronic warfare, communication systems and microwave consumer electronics. The MSAG MMIC technology based on the MESFET has demonstrated state-of-the-art performance for narrow band and broadband applications up to 18 GHz. A broadband power amplifier at X/Ku-band has demonstrated over 3W power output with a minimum PAE of 24% over a 7 GHz bandwidth.

References


Table 1. Status of Narrowband High-Efficiency MESFET Power ICs

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>Number of Stages</th>
<th>P_out (W)</th>
<th>PAE (%)</th>
<th>Gain (dB)</th>
<th>Company</th>
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<tbody>
<tr>
<td>1.3</td>
<td>1</td>
<td>9.0</td>
<td>52</td>
<td>16</td>
<td>ITT</td>
</tr>
<tr>
<td>5.0</td>
<td>1</td>
<td>5.0</td>
<td>60</td>
<td>9</td>
<td>ITT</td>
</tr>
<tr>
<td>5.5</td>
<td>1</td>
<td>1.7</td>
<td>70</td>
<td>8</td>
<td>ITT</td>
</tr>
<tr>
<td>8.5</td>
<td>2</td>
<td>3.2</td>
<td>52</td>
<td>14</td>
<td>Hughes</td>
</tr>
<tr>
<td>10.0</td>
<td>1</td>
<td>5.0</td>
<td>48</td>
<td>7</td>
<td>ITT</td>
</tr>
<tr>
<td>10.0</td>
<td>1</td>
<td>6.0</td>
<td>44</td>
<td>6</td>
<td>ITT</td>
</tr>
<tr>
<td>11.5</td>
<td>2</td>
<td>3.0</td>
<td>42</td>
<td>12</td>
<td>ITT</td>
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<tr>
<td>14.0</td>
<td>1</td>
<td>4.0</td>
<td>36</td>
<td>5</td>
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Table 2. Status of Broadband MESFET Power ICs

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>Configuration</th>
<th>Number of Stages</th>
<th>Gain (dB)</th>
<th>P_out (W)</th>
<th>PAE (%)</th>
<th>Company</th>
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<tbody>
<tr>
<td>1.5-9.0</td>
<td>Reactive Match</td>
<td>2</td>
<td>5</td>
<td>0.5</td>
<td>14</td>
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<td>Reactive Match</td>
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<td>17</td>
<td>1.0</td>
<td>25</td>
<td>M/A-COM</td>
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<tr>
<td>2.0-8.0</td>
<td>Distributed</td>
<td>1</td>
<td>5</td>
<td>1.0</td>
<td>--</td>
<td>Raytheon</td>
</tr>
<tr>
<td>2.0-20.0</td>
<td>Distributed</td>
<td>1</td>
<td>4</td>
<td>0.8</td>
<td>15</td>
<td>TI</td>
</tr>
<tr>
<td>3.5-8.0</td>
<td>Reactive Match</td>
<td>2</td>
<td>10</td>
<td>2.0</td>
<td>20</td>
<td>Raytheon</td>
</tr>
<tr>
<td>6-17</td>
<td>Dist./Reactive</td>
<td>4</td>
<td>16</td>
<td>0.8</td>
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<td>Raytheon</td>
</tr>
<tr>
<td>6-20</td>
<td>Distributed</td>
<td>1</td>
<td>11</td>
<td>0.25</td>
<td>--</td>
<td>HP</td>
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<tr>
<td>7-11</td>
<td>Reactive Match</td>
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<td>14</td>
<td>4.0</td>
<td>35</td>
<td>ITT</td>
</tr>
<tr>
<td>7-10.5</td>
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<td>12.5</td>
<td>3.0</td>
<td>35</td>
<td>Hughes</td>
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<td>7.7-12.2</td>
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<td>Hughes</td>
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<tr>
<td>9-14</td>
<td>Reactive Match</td>
<td>2</td>
<td>9.0</td>
<td>4.0</td>
<td>37</td>
<td>ITT</td>
</tr>
<tr>
<td>10-17</td>
<td>Reactive Match</td>
<td>1</td>
<td>4.0</td>
<td>3.0</td>
<td>24</td>
<td>ITT</td>
</tr>
<tr>
<td>12-16</td>
<td>Reactive Match</td>
<td>3</td>
<td>18</td>
<td>1.8</td>
<td>18</td>
<td>Hughes</td>
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<tr>
<td>14-33</td>
<td>Distributed</td>
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<td>4</td>
<td>0.1</td>
<td>--</td>
<td>Raytheon</td>
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### Table 3. Broadband Power Amplifier Approaches

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<th>BW</th>
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<th>Parameters</th>
<th>P&lt;sub&gt;0&lt;/sub&gt;</th>
<th>Gain</th>
<th>VSWR</th>
<th>Comments</th>
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<tbody>
<tr>
<td>Balanced*</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
<td>Excellent</td>
<td>Excellent</td>
<td>Recommended over less than octave BW and high power</td>
</tr>
<tr>
<td>Distributed</td>
<td>Excellent</td>
<td>Poor</td>
<td>Fair</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
<td>Recommended over octave BW and medium power</td>
</tr>
<tr>
<td>Feedback</td>
<td>Excellent</td>
<td>Poor</td>
<td>Fair</td>
<td>Good</td>
<td>Fair</td>
<td>Fair</td>
<td>Recommended for medium power</td>
</tr>
<tr>
<td>Reactive/Resistive</td>
<td>V. Good</td>
<td>Excellent</td>
<td>Excellent</td>
<td>Good</td>
<td>Good Input Poor Output</td>
<td>Recommended over less than two octave BW and high power</td>
<td></td>
</tr>
<tr>
<td>Pushpull</td>
<td>Fair</td>
<td>Excellent</td>
<td>Excellent</td>
<td>Excellent</td>
<td>Poor</td>
<td>Low loss baluns are not yet developed</td>
<td></td>
</tr>
<tr>
<td>Combiner using uneven line lengths</td>
<td>Good</td>
<td>V. Good</td>
<td>V. Good</td>
<td>Good</td>
<td>V. Good</td>
<td>Recommended over less than octave BW and high power</td>
<td></td>
</tr>
</tbody>
</table>

*On 3 mil GaAs substrate Lange coupler has about 0.7 dB loss at 18 GHz*

### Table 4. Effect of Device Uniformity Across the Wafer on 4W Broadband IC Performance

<table>
<thead>
<tr>
<th>PCM FET Parameter</th>
<th>Experiment</th>
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<td>Average I&lt;sub&gt;oss&lt;/sub&gt;/mm (mA)</td>
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</tr>
<tr>
<td>SD I&lt;sub&gt;oss&lt;/sub&gt; (mA)</td>
<td>331</td>
</tr>
<tr>
<td>Average pinch-off voltage (-V)</td>
<td>2.61</td>
</tr>
<tr>
<td>SD V&lt;sub&gt;p&lt;/sub&gt; (-V)</td>
<td>0.07</td>
</tr>
<tr>
<td>No. of ICs tested</td>
<td>3</td>
</tr>
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</table>

| Average power output (dBm) @ 13.5 GHz | 35.9 | 35.4 | 34.7 |
| Average PAE (%) @ 13.5 GHz | 32.6 | 31.0 | 27.4 |
Fig. 1  Performance of Single-Chip Power MMIC Amplifiers

Fig. 3  Microphotograph of 10-Watt C-Band Power MMIC

Fig. 2  MMIC Amplifier Design Flow Diagram
Fig. 4   Measured P out vs. Pin of 10W Power Amplifier

Fig. 5   Broadband Power Amplifier Configurations
Fig. 6  Fractional Bandwidth as a Function of Impedance Transformation Ratio

Fig. 7  CALMA Layout of the Single Stage Ku-Band Class-B Power MMIC Amplifier Chip
Fig. 8 Measured Performance of 3 Chips of Ku-Band 4-W MMIC Amplifier

Fig. 9 Photograph of the 2-Stage X-Band 4-W Power Amplifier Chip
Fig. 10  X/Ku-Band 4-W Broadband Amplifier

Fig. 11  Combining Efficiency vs Combiner Loss for Various Gain Values
UNEQUAL LINE LENGTH COMBINER

- MMIC CHIP REFLECTIONS DO NOT ADD IN PHASE
- REDUCES INPUT AND OUTPUT RETURN LOSS
- PROVIDES BETTER MATCHING

Fig. 12  4-Way Broadband Planar Combiner with Good VSWR

Fig. 13  Photograph of a Pair of 4-Way Traveling Wave Divider/Combiners in a Back to Back Configuration and Mounted in a Test Fixture Constructed to simulate the Final Package Environment
Fig. 14 Measured and Predicted Insertion Loss and Return Loss of a Pair of TWD/Cs in a Back to Back Configuration

Fig. 15 X/Ku-Band 12-W Broadband Amplifier
Fig. 16  Measured Performance of a 12W MMIC Based Power