Two-capacitor Transformer Winding Capacitance Models for Common-Mode EMI Noise Analysis in Isolated DC-DC Converters

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Abstract—For isolated DC-DC power converters, the inter-winding parasitic capacitance of the transformer is usually one of the main paths for common-mode (CM) noise. In order to simplify the CM noise analysis, this paper proposes a two-capacitor transformer winding capacitance model. The model is derived based on general conditions so it can be applied to different isolated converter topologies. A measurement technique is also proposed to obtain the lumped capacitance for the model. The CM noise models of several isolated converter topologies are analyzed with the proposed two-capacitor transformer winding capacitance model to achieve simplicity. Finally, the proposed transformer winding capacitance model and measurement technique are verified by simulations and experiments.

Keywords—Common-mode, electromagnetic interference, transformer winding capacitance model, isolated power converters.

NOMENCLATURE

\( v_P \) Primary voltage of the transformer [V].
\( v_S \) Secondary voltage of the transformer [V].
\( \Delta v_P \) Voltage difference between two adjacent sections of the primary winding [V].
\( \Delta v_S \) Voltage difference between two adjacent sections of the secondary winding [V].
\( L_{LK} \) Transformer leakage inductance [H].
\( v_{Pi} \) The voltage of section \( i \) on primary winding [V].
\( v_{Si} \) The voltage of section \( j \) on secondary winding [V].
\( C_{PSi} \) Inter-winding parasitic capacitance between primary section \( i \) and secondary section \( j \) [F].
\( C_{PSk} \) Primary intra-winding parasitic capacitance between primary section \( k \) and \( l \) [F].
\( C_{SmSn} \) Secondary intra-winding parasitic capacitance between secondary section \( m \) and \( n \) [F].
\( C_O \) The drain/collector to ground/heatsink parasitic capacitance of the MOSFET/IGBT [F].
\( C_D \) The cathode to ground/heatsink parasitic capacitance of the diode [F].
\( C_{OD} \) A combination of \( C_O \) and \( C_D \) [F].

I. INTRODUCTION

Developing an accurate, simple and efficient common mode (CM) noise model for DC-DC converters is very important for the analysis, prediction and reduction of CM noise.

For isolated DC-DC power converters, the inter-winding parasitic capacitance of the transformer is usually one of the main paths for CM noise [1] [2] [3] [4] [5] [6]. A high frequency (HF) transformer model is therefore the key for characterizing the CM noise. Several HF transformer modeling and parameter extraction methods have been proposed. However, many of them are not well suited for CM noise analysis. Some [7] [8] [9] [10] [11] pay little interest in the distribution of inter-winding capacitances when building the model. Their applications are mainly for examining the differential mode (DM) circuit dynamic behavior. Others are either too complicated [12] [13] [14] [15] [16] [17] [18] [19] or vague [20] [21] [22] in how to determine the parasitic capacitances for different transformer structures thus lack the ability for derivation of CM noise reduction techniques.

In order to facilitate the CM noise analysis, [3] [4] [6] use equivalent lumped capacitances as a CM noise model to represent a real transformer which has distributed parasitic capacitances. One basic rule for the derivation of the lumped capacitance model is that the displacement current generated by the model must be equal to the actual transformer [4] [6]. As a result, the examination of the transformer’s physical structure is unavoidable in all previous works. Due to the complexity of a real transformer, two assumptions are generally made to simplify the analysis. One assumption is that the voltage potential varies linearly along the windings; the other assumption is the parasitic capacitance between two adjacent windings is evenly distributed. Both assumptions linearize and simplify the displacement current calculation for a real transformer.

The modeling technique above works well for some transformers, especially for the transformers with spiral wire windings. However, it also has some issues. Firstly, it is unclear why the displacement current instead of energy should be conserved during the model derivation. This actually defines a condition for the method to be used. Secondly, the two important assumptions needed for the derivation cannot be well held for some transformer structures, especially for planar transformers with non-uniform winding layer profiles. Therefore, a new technique to extract the equivalent lumped capacitances without using these assumptions needs to be developed. Furthermore, the equivalent lumped capacitance model should be generalized for different isolated converter topologies. [6] did part of this work and is able to provide a general transformer model. The transformer winding capacitance is quantified and represented by four capacitances. However, the model derivation in the paper is still based on the two assumptions so it cannot be applied to a more general case.
This paper proposes a generalized two-capacitor transformer winding capacitance model for isolated power converters. Section II discusses existing techniques for solving the CM EMI issues of the isolated power converters. Section III derives the general constraints for the equivalent lumped capacitance transformer model using both the energy conservation rule and the displacement current conservation rule. A two-capacitor transformer winding capacitance model is then proposed based on the constraints of general applications. Section IV applies the proposed transformer model to different isolated converter topologies to demonstrate its flexibility and ability in the simplification of CM noise models. Section V proposes a measurement technique to extract the equivalent capacitances for the model. In Section VI, both a LLC resonant converter and a flyback converter are used to validate the proposed transformer model.

II. EXISTING CM NOISE ANALYSIS METHODOLOGIES FOR ISOLATED POWER CONVERTERS

The inter-winding capacitance of a transformer is one of the major paths for CM noise. This is mainly because of the high displacement currents due to the \( \frac{dv}{dt} \) added to the parasitic capacitances in the transformer. Additionally, interleaved winding structure is usually used to reduce winding loss. This increases the parasitic capacitance between the primary and secondary windings [4]. Furthermore, transformers tend to achieve low profiles and high power densities, so spiral wire windings may not be preferred. On the other hand, planar transformer is preferred since it is able to provide multiple benefits including low profile, good thermal characteristic, good repeatability and etc. [17]. Nevertheless, it has higher winding capacitance which generates higher CM noise than spiral wire winding transformer due to its closely stacked layers and intrinsically large layer surface areas.

There are two popular approaches to reduce the CM noise flowing through transformers [2] [6]. The basic principle of the first approach is to make sure that the adjacent primary and secondary winding layers have the same voltage distributions. It is assumed that the inter-winding parasitic capacitances of the transformer are evenly distributed between these two adjacent winding layers, zero \( \frac{dv}{dt} \) can be maintained over these capacitances so no CM current is generated if there is no other parasitic capacitance between the primary and secondary winding layers.

![Transformer Structure](image)

(a) A typical transformer structure optimized for CM noise reduction and (b) the voltage distributions along winding layers.

Fig. 1 (a) shows a transformer example for the flyback converter in Fig. 5 (a) [2]. Winding AB is primary and winding CD is secondary. The primary layer and the secondary layer C-N1 have identical voltage distributions as shown in Fig. 1 (b). It should be noted that line impedance stabilization networks (LISNs) are treated as short circuit for CM noise since their CM impedance is small compared with the impedance of transformer’s parasitic capacitances. Because of this, both A and C terminals are equivalently connected to ground. \( v_{d} \) is approximately equal to \( v_{C} \). So the \( \frac{dv}{dt} \) and the CM current between the two layers is zero. Apparently, the condition for this approach is that the voltage potential difference \( v_{A} + v_{C} \) is always constant. For any power converter topologies meeting this condition, the approach can be applied to reduce the CM noise flowing through the transformer.

Following this rule, it has been identified that, besides flyback converter, this approach can also be applied to forward converter (Fig. 6), push-pull converter (Fig. 8) and half-bridge LLC resonant converter (Fig. 9). However, for two-switch forward converter (Fig. 7) and full-bridge LLC resonant converter (Fig. 10), further examination is needed. It can be identified by the generalized equivalent noise source (ENS) method [6] that this approach does not work for any full-bridge converters with phase-shift control.

The effectiveness of the first approach is further limited when CM noise has more paths other than the transformer parasitic capacitance, e.g. the drain/collector to ground/heat sink parasitic capacitance of the MOSFET/IGBT. Furthermore, this approach only considers the parasitic capacitance between two adjacent layers. In some cases, when two layers are separated by a layer of thin or sparse winding such as the reset winding, the parasitic capacitance between these two layers cannot be ignored. [5] considers these limitations and proposes a generalized CM current cancelation (GCMCC) technique which considers the CM noise from all CM paths. The technique was implemented on a forward converter and it also suggests that some transformer structures have better CM noise performance than others. However, it lacks the ability to predict the best transformer structure before the prototype is developed or its parasitic capacitances can be measured. Moreover, the first approach cannot be implemented in highly interleaved winding structures. [4] analyzes a half-bridge LLC resonant converter with a fully interleaved planar transformer. Instead of implementing the first approach, the paper uses balance technique to reduce the CM noise.

The second approach is to first develop a transformer parasitic capacitance model based on its physical structure. Based on this model, various CM noise cancellation techniques, such as the balance technique [3] [4] [23], can be developed. [3] studies the CM noise balance technique for a two-switch forward converter based on its transformer parasitic capacitance model. According to displacement current conservation rule, [6] summarized the process to extract parasitic capacitance based on transformer physical structure.

Despite their effectiveness, [2] [3] [4] [5] [6] all derived their key equations based on two important assumptions: a) the voltage potential varies linearly along the windings; b) the parasitic capacitances only exist between the adjacent layers and they are evenly distributed. It will be shown later that the displacement current conservation rule and the two assumptions limit the applications of using the existing lumped transformer winding capacitance model to reduce CM noise so a more
generalized approach needs to be developed.

III. TRANSFORMER WINDING CAPACITANCE MODEL

A good lumped winding capacitance model for a transformer is important for both CM noise simulation and analysis. Both [3] and [6] uses the displacement current conservation rule to develop lumped winding capacitance model for EMI analysis. First, it is unclear under what conditions, the displacement current conservation rule holds for CM noise analysis. Second, it will be shown later that under some conditions, energy conservation rule instead of displacement current conservation rule should be used to derive transformer’s lumped winding capacitance model. In this section, lumped winding capacitance models will be derived for transformers under general conditions. The conditions for both rules will be identified.

A. Transformer Winding Capacitance Model Based on Energy Conservation

Fig. 2 (a) shows a two-winding transformer including its leakage inductances, inter- and intra-winding capacitances. Core loss and copper loss are not modeled as they are not important for EMI analysis. \( v_p \) and \( v_S \) are the primary and secondary voltages. \( L_{j,k} \), \( L_{j,k} \) and \( L_{j,k} \) are primary and secondary leakage inductances respectively. If the primary winding is separated to \( N \) sections from terminal \( A \) to \( B \), and secondary winding is separated to \( M \) sections from terminal \( C \) to \( D \) with different voltages, the inter-winding parasitic capacitance between primary section \( i \) and secondary section \( j \) is \( C_{psj} \), where \( j=1,2,\ldots,N \) and \( i=1,2,\ldots,M \). Similarly, \( C_{ips} \) is defined as the primary intra-winding capacitance between primary sections \( i \) and \( j \), and \( C_{smn} \) is defined as the secondary intra-winding capacitance between secondary sections \( m \) and \( n \), where \( k \) or \( l=1,2,\ldots,N \), and \( m \) or \( n=1,2,\ldots,M \).

The energy stored in transformer’s inter-winding capacitances is:

\[
W_1 = \sum_{i=1}^{N} \sum_{j=1}^{M} \frac{1}{2} C_{psj} \left( v_{pi} - v_{sj} \right)^2
\]

The energy stored in primary intra-winding capacitances is:

\[
W_2 = \sum_{i=1}^{N} \sum_{j=1}^{M} \frac{1}{2} C_{ips} \left( v_{pi} - v_{pj} \right)^2
\]

The energy stored in secondary intra-winding capacitances is:

\[
W_3 = \sum_{m=1}^{M} \sum_{n=1}^{M} \frac{1}{2} C_{smn} \left( v_{sm} - v_{sn} \right)^2
\]

And the total energy stored within parasitic winding capacitance is:

\[
W = W_1 + W_2 + W_3
\]

Based on equations (1)-(7), (8) can be represented as:

\[
W = \frac{1}{2} k_1 (v_B - v_C)^2 + \frac{1}{2} k_2 v_p^2 + \frac{1}{2} k_4 (v_B - v_C)^2 + \frac{1}{2} k_3 v_S^2 + \frac{1}{2} k_6 v_P v_S
\]

where:

\[
k_1 = \sum_{i=1}^{N} \sum_{j=1}^{M} C_{psj}
\]

\[
k_2 = \sum_{i=1}^{N} \sum_{j=1}^{M} \frac{N-i}{N-1} + \sum_{i=1}^{N} \sum_{j=1}^{M} \frac{(i-k)^2}{N-1}
\]

\[
k_3 = \sum_{i=1}^{N} \sum_{j=1}^{M} \frac{M-j}{M-1} + \sum_{i=1}^{N} \sum_{j=1}^{M} \frac{(n-m)^2}{M-1}
\]

\[
k_4 = 2 \sum_{i=1}^{N} \sum_{j=1}^{M} \frac{N-i}{N-1}
\]

\[
k_5 = 2 \sum_{i=1}^{N} \sum_{j=1}^{M} \frac{M-j}{M-1}
\]

\[
k_6 = \sum_{i=1}^{N} \sum_{j=1}^{M} \frac{N-i}{N-1} \frac{M-j}{M-1}
\]

The effect of leakage inductances is ignored in the analysis above as they significantly complicate the energy calculation. Because of this, the analysis in this paper applies to all the transformers with small leakage inductances. After leakage inductances are ignored, \( v_p \) and \( v_S \) meet condition:

\[
v_p = n v_S
\]

Substituting (16) into (9) yields:

\[
W = \frac{1}{2} k_1 (v_B - v_C)^2 + \frac{1}{2} k_4 (v_B - v_C)^2 + \frac{1}{2} k_3 v_S^2
\]

where:

\[
k_4 = nk_1 + k_3
\]

\[
k_5 = nk_2 + k_3 + nk_6
\]

Constants \( k_4 \), \( k_5 \) and \( k_6 \) are determined by transformer winding structure. (17) shows that there are only two independent transformer terminal voltage differences: \( v_p-v_C \) and \( v_S \) in the calculation of the total energy stored in parasitic winding capacitance. This is reasonable as for all of the four terminal voltage differences \( v_P, v_S, v_B-v_C \) and \( v_P-v_D \), there are two

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constraints: (16) and the KVL, \( v_P-v_Q+(v_B-v_C)-(v_A-v_D)=0 \), so there are only two independent terminal voltage differences.

The simplest transformer winding capacitance model is the one with the least number of lumped capacitances. The derivation of the simplest model starts from a commonly used six-capacitor model in Fig.2 (b). The total energy stored in parasitic capacitances is:

\[
W = \frac{1}{2} \left( C_{AD} + C_{BD} + C_{AC} + C_{BC} \right) (v_A - v_C)^2 \\
+ \left( (n-1)C_{AD} + nC_{AC} - C_{BD} \right) (v_B - v_C) v_S \\
+ \frac{1}{2} \left[ (n-1)^2 C_{AD} + n^2 C_{AC} + C_{BD} + n^2 C_{AB} + C_{CD} \right] v_S^2
\]

(20)

The corresponding coefficients of (17) and (20) should be equal:

\[
k_1 = C_{AD} + C_{BD} + C_{AC} + C_{BC} \\
\frac{1}{2} k_2 = (n-1)C_{AD} + nC_{AC} - C_{BD} \\
k_3 = (n-1)^2 C_{AD} + n^2 C_{AC} + C_{BD} + C_{INTRA}
\]

(21)

Equation (21) derived from the energy conservation is therefore valid. The transformer winding capacitance can be modeled with displacement current conservation. The other two capacitances can be set to zero. For example, if \( C_{AC} \) and \( C_{BC} \) are set to zero, \( k_1 = C_{AD} + C_{BD} \).

C. Discussions on the Results from Two Rules

Comparing (21) and (27), the first two constraints are identical and they are determined by the inter-winding capacitances only. The energy conservation results in one more constraint which reflects the effect of intra-winding capacitance. So it can correctly characterize both inter and intra winding capacitances, while the displacement current conservation cannot characterize the intra-winding capacitance.

Although CM noise current is directly related to the inter-winding capacitance, depending on the converter topologies, the intra-winding capacitance may influence the CM noise by influencing the waveforms of voltage \( v_P, v_B, v_C \) and \( v_D \). Equation (21) derived from the energy conservation is therefore more preferred for CM noise analysis and simulations than (27) derived from displacement current conservation for some converter topologies.

When an independent voltage source is directly connected to a transformer terminal, the intra-winding capacitances have no influence to the voltage waveform of that terminal since it is in parallel with the voltage source.

D. Two-capacitor Transformer Winding Capacitance Model

Based on the analysis above, when two conditions below are met, the transformer winding capacitance can be modeled with two capacitors.

1) The transformer’s leakage inductance is small so its effect can be ignored.

2) At least one winding of the transformer are connected to an equivalent independent voltage source. This source can be the equivalent voltage source used to substitute nonlinear switches [23].

Condition 1) ensures that the three constraints derived by energy conservation, in (21) are valid. The transformer winding capacitance is able to be represented with one intra-winding capacitance and two inter-winding capacitances. Condition 2) ensures that the intra-winding capacitance is in parallel with an
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Independent voltage source so it can be removed in noise analysis. Therefore, only two inter-winding capacitors are needed to represent transformer winding capacitance. The extraction of the two inter-winding capacitances will be discussed later.

![Diagram of possible two-capacitor CM winding capacitance models for a two-winding transformer.](image)

**Fig. 3.** Six possible two-capacitor CM winding capacitance models for a two-winding transformer.

As shown in Fig. 3, there are 6 possible two-capacitor winding capacitance models for a two-winding transformer. For a center-tapped three-winding transformer, its two-capacitor winding capacitance model can be derived based on the same process as a two-winding transformer. The resulting models can be found in Fig. 4. The total number of possible models is \( C^2 = 6 \times 5 / 2 = 15 \). Since the center-tapped three winding transformer can be treated as a two-winding transformer with one added terminal in the center, two capacitances are still enough for the model.

**E. Influence of Leakage Inductance on the Model**

The influence of leakage inductance becomes significant when the frequency is high due to its increased impedance. Therefore, the boundary frequency below which the proposed transformer model is good for CM EMI analysis can be approximately evaluated and calculated based on the resonant frequency between the leakage inductance and the total inter-winding parasitic capacitance of the transformer \( k_j \). In Fig. 2(a), under normal conditions, \( L_{kk} = L_{kk'} \), \( L_{kk} = L_{kk'} \), the resonant frequency between the leakage inductance and \( k_j \) is calculated as:

\[
f_{CM} \approx \frac{1}{\sqrt{2 \pi \sqrt{(L_{kk} + L_{kk'})k_j}}}
\]

(28)

Below \( f_{CM} \), the model is good for CM noise analysis because the leakage inductance’s impedance can be ignored as it is much smaller than \( k_j \)'s impedance. Above \( f_{CM} \), the model becomes less effective as the impedance of the leakage inductance is dominant on the CM noise’s path in the transformer. In many cases, \( f_{CM} \) is high enough to cover most of the concerned frequency range (150kHz to 30MHz). Sometimes, circuit designers intentionally increase transformer’s leakage inductance so it can be used as a resonant inductance in resonant converters. If that is the case, researchers should always use (28) to check if the proposed model can still be applied to CM noise analysis.

**IV. APPLICATIONS OF THE TWO-CAPACITOR TRANSFORMER WINDING CAPACITANCE MODEL TO CM NOISE ANALYSIS**

The advantage of the proposed two-capacitor transformer winding capacitance model lies in its flexibilities for the analysis and cancellation of the CM noise caused by transformer winding capacitances. Along with the substitution theory which was first used for noise analysis in [8], it has the ability to greatly simplify the CM noise model for isolated power converters.

The applications of the two-capacitor winding capacitance model to the CM analysis of the conventional isolated power converters are shown from Fig. 5 to Fig. 10. In these figures, \( C_Q \) represents the drain/collector to ground/heatsink parasitic capacitance of the MOSFET/IGBT. \( C_D \) represents the cathode to ground/heatsink parasitic capacitance of the diode. \( C_{QD} \) includes both \( C_Q \) and \( C_D \).

The derivation of the CM noise models based on two-capacitor winding capacitance model for the analysis of the CM noise caused by transformer winding capacitances follows 7 steps below.

1) Substitute nonlinear semiconductor devices with either equivalent voltage sources or currents sources using substitution theory. The voltage and current sources shall have the same time domain waveforms as the originals. Using either voltage sources or currents sources depends on the convenience in noise analysis [5]. The input and output bulk DC capacitors are treated as short circuit because they have very small impedance to CM noise.

2) If one transformer winding is paralleled with a voltage source, replace all other windings with controlled voltage sources because the winding voltages depend on transformer turn ratios.

3) Simplify the model by removing all components that are in parallel with the voltage sources or in series with current sources.

4) Use one of the models that most simplifies the CM noise analysis in Fig. 3 or Fig. 4 to replace the original transformer.

5) Analyze the CM noise generated by every voltage source and current source based on superposition theory.

6) Remove the parasitic capacitances that do not contribute to the CM noise flowing through LISNs by analyzing the circuit derived from step 1) to 5).

7) Analyze CM noise based on the resultant CM noise models developed from step 1) to 6).

Step 4 is very important as it is directly related to CM noise analysis and cancellation techniques. This paper will employ examples to show how to use the two-capacitor transformer winding capacitance model to simplify the CM noise analysis. Based on the developed CM EMI model, it is easy to derive techniques for CM noise cancellation.
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Fig. 5. CM model for a flyback converter: (a) converter circuit, (b) substitute nonlinear devices with voltage and current sources, (c) final CM model.

Fig. 6. CM model for a forward converter: (a) converter circuit, (b) substitute nonlinear devices with voltage and current sources, (c) final CM model.

Fig. 7. CM model for a two-switch forward converter: (a) converter circuit, (b) substitute nonlinear devices with voltage and current sources, (c) final CM model.

Fig. 8. CM model for a push-pull converter: (a) converter circuit, (b) substitute nonlinear devices with voltage and current sources, (c) final CM model.

Fig. 9. CM model for a half-bridge LLC resonant converter: (a) converter circuit, (b) substitute nonlinear devices with voltage and current sources, (c) final CM model.

Fig. 10. CM model for a full-bridge LLC resonant converter: (a) converter circuit, (b) substitute nonlinear devices with voltage and current sources, (c) final CM model.
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A. Flyback Converter

Following steps 1 and 2, the flyback converter in Fig. 5 (a) can be transformed to Fig. 5 (b). Following steps 3-6, \( i_{D1} \) does not contribute to CM noise and final CM model is derived in Fig. 5 (c). In step 4, the model 3 in Fig. 3 is selected as transformer model because with this model, \( V_{Q1} \) on the secondary does not contribute to CM noise. Furthermore, there is no current flowing through \( C_{AC} \) as the LISNs' impedance is much smaller than that of \( C_{Q1} \). The condition for CM noise cancellation is \( C_{BC} = -C_{Q1} \). Negative capacitance is mathematically possible in transformer models.

B. Forward Converter

Following steps 1 and 2, the forward converter in Fig 6 (a) can be transformed to Fig. 6 (b). Following steps 3-6, \( i_{D1}, V_{Q2} \) and \( i_{D3} \) do not contribute to CM noise, and final CM model is derived in Fig. 6 (c). In Fig. 6 (c), since \( C_{AD} \) and \( C_{BD} \) are both connected to the secondary ground, \( V_{Q1} \) on the secondary does not contribute to CM noise. The voltages between N and A, C and N are both \( V_{Q1} \). If \( C_{BD}=C_{Q1}, C_{AD}=C_{CD} \), the CM currents can be canceled.

C. Two-Switch Forward Converter

Following steps 1 and 2, the two-switch forward converter in Fig 7 (a) can be transformed to Fig. 7 (b). Following steps 3-6, \( i_{D1}, i_{D2}, i_{D3} \) and \( V_{Q4} \) do not contribute to CM noise and the final CM model is derived in Fig. 7 (c). The final CM model is similar to that of the forward converter model in Fig. 6 (c). Based on the operation principle of two-switch forward converter, ideally, \( V_{Q1} \) and \( V_{Q2} \) have identical waveforms. If \( C_{D2}=C_{Q1}, C_{AD}=C_{BC} \), the CM currents can be canceled.

D. Push-pull Converter

Although the topology in Fig. 8 (a) is very different from the forward converter in Fig. 6 (a), the final CM model for push-pull converter with the two-capacitance transformer model in Fig. 8 (c) is similar to that of a forward converter. The condition to cancel CM noise is \( C_{Q1}=C_{Q2}, C_{AE}=C_{CE} \).

E. Half-bridge LLC Resonant Converter

For the half-bridge LLC resonant converter in Fig. 9 (a), following steps 1 and 2, the CM noise model in Fig. 9 (b) can be derived. Following steps 3-6, \( i_{Q5} \) does not contribute to CM noise and the final CM model is derived in Fig. 9 (c). As shown in Fig. 9 (c), for the half-bridge LLC resonant converter, the two capacitances \( C_{BE} \) and \( C_{BC} \) are selected to take advantage of two identical secondary voltages and the transformer primary voltage \( V_{Q1} \) can be ruled out in CM noise analysis. If the CM noise generated by \( C_{Q1} \) can be ignored, the condition for CM noise cancellation is \( C_{BE}=C_{CB} \).

F. Full-bridge LLC Resonant Converter

For the full-bridge LLC resonant converter in Fig. 10 (a), following steps 1 and 2, the CM noise model in Fig. 10 (b) can be derived. Following steps 3-6, \( i_{Q5} \) and \( i_{Q6} \) do not contribute to CM noise and the final CM model is derived in Fig. 10 (c). Theoretically, based on the operating principle of full-bridge LLC resonant converters, \( V_{Q1}=V_{Q2} \). It is also assumed that the switching frequency is equal or very close to the resonant frequency, so \( V_{Q1}=V_{Q2} \). Because the output is grounded, independent and dependent voltage sources \( V_{Q1} \) do not contribute to CM noise. \( C_{Q1} \) and \( C_{Q2} \) are shorted by the output grounding. Based on these relationships, the condition for CM cancellation is \( C_{Q1}=C_{Q2} \) and \( C_{AD}=C_{BD} \).

It should be pointed out that the converter outputs in Figs. 5 -10 are grounded. If they are not grounded, the CM noise analysis and the conditions for CM noise cancellation could be different. The techniques developed in this paper still apply.

V. EXTRACTION OF CAPACITANCES FOR TWO-CAPACITOR TRANSFORMER WINDING CAPACITANCE MODELS

In this section, the relationship of different transformer models in Fig. 3 and Fig. 4 will be first discussed. An extraction technique is proposed to determine the capacitances in the transformer models.

A. The Relationship of Different Two-capacitor Transformer Winding Capacitance Models

Since the intra-winding capacitance of the transformer can be removed in CM EMI analysis when an independent voltage source is added to one terminal of the transformer, the two-capacitor transformer winding capacitance model only characterize the inter-winding capacitance; that is to say, all the models in Fig. 3 and Fig. 4 are only limited by the first two constraints in (21). These models lead to identical CM noise. Displacement current rule can be used to find their relationships since it has enough information in defining the inter-winding capacitance.

If models 2 and 11 in Fig. 4 are taken as examples, the displacement CM currents derived from the two models are:

\[
\begin{align*}
\frac{dC_{CM}}{dt} &= C_{AD} \frac{dv_{AD}}{dt} + C_{BD} \frac{dv_{BD}}{dt} \\
\frac{dC_{CM}}{dt} &= C_{BE} \frac{dv_{BE}}{dt} + C_{BC} \frac{dv_{BC}}{dt}
\end{align*}
\]

(29)

(30)

If the turn ratio of the transformer is \( r:1:1 \), \( v_{AD}, v_{BE} \) and \( v_{BC} \) can be expressed as:

\[
\begin{align*}
v_{AD} &= v_{AB} + v_{BD} = n v_{BD} + v_{BD} \\
v_{BE} &= v_{BD} - v_{ED} \\
v_{BC} &= v_{BD} + v_{ED} = v_{BD} + v_{ED}
\end{align*}
\]

(31)

(32)

(33)

Substituting (31)-(33) into (29) and (30) yields:

\[
\begin{align*}
\frac{dC_{CM}}{dt} &= (C_{AD} + C_{BD}) \frac{dv_{BD}}{dt} + nC_{AD} \frac{dv_{ED}}{dt} \\
\frac{dC_{CM}}{dt} &= (C_{BE} + C_{BC}) \frac{dv_{BD}}{dt} + (C_{BE} - C_{BC}) \frac{dv_{ED}}{dt}
\end{align*}
\]

(34)

(35)

By comparing the coefficients of (34) and (35), the relationship of the capacitances in these two models is:

\[
\begin{align*}
C_{BE} &= (1-n)C_{AD} + C_{BD} \\
C_{BC} &= (1+n)C_{AD} + C_{BD}
\end{align*}
\]

(36)

If \( C_{BD}/C_{AD} = h \),

\[
\frac{C_{BC}}{C_{BE}} = h + 1 + n \
\frac{C_{BE}}{C_{BE}} = h + 1 + n
\]

(37)

The capacitance relationship of other models can be derived similarly. If the capacitances of one model are extracted, the capacitances of all other models can be calculated.
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B. Extraction of Capacitances for Transformer Models

Equation (37) indicates that if the capacitance ratio \( C_{BD}/C_{AD} = h \) can be directly measured; the ratio of \( C_{BC} \) to \( C_{BE} \) can be calculated from \( n \) and \( h \). Similarly, the capacitance ratio of any two capacitances in other models in Fig. 4 can also be derived.

\[
\begin{align*}
C_{BD} &= k_1 \frac{v_{AD}}{v_g} \\
C_{AD} &= k_1 \frac{v_{DB}}{v_g}
\end{align*}
\]

(38)

Otherwise the probe capacitance should be considered in the calculation. The capacitances of all other models can be calculated based on their relationships, which can be derived following the procedure in Section V A with \( C_{AD} \) and \( C_{BD} \).

The model 2 in Fig. 4 is taken as an example for the proposed parasitic capacitance extraction technique in Fig. 11. In Fig. 11 (a), primary terminals and secondary terminals are first shorted. The total primary to secondary capacitance \( k_1 \), which is defined in (21) and (27), is then measured using an impedance analyzer. In Fig. 11 (b), a signal generator is added to the primary winding. The voltage \( v_{AD} \) between terminals A and D and the voltage \( v_{DB} \) between terminals D and B are measured using an oscilloscope or a voltmeter. If the capacitance of the voltage probes of the oscilloscope or the voltmeter can be ignored, \( C_{AD} \) and \( C_{BD} \) can be solved by (38),

\[
\begin{align*}
C_{BD} &= \frac{k_1}{k_1} v_{AD} \\
C_{AD} &= k_1 \frac{v_{DB}}{v_g}
\end{align*}
\]

Fig. 11. Extract the capacitances for transformer winding capacitance model: (a) measure the total primary to secondary capacitance \( k_1 \), and (b) measure the voltage ratio between \( v_{AD} \) and \( v_{DB} \).

For the CM model of a half-bridge LLC converter in Fig. 12, the capacitances \( C_{AD} \) and \( C_{BD} \) can also be extracted by directly measuring the voltage \( v_{AD} \) between terminals A and D and the voltage \( v_{DB} \) between terminals D and B at working conditions if \( C_{Q1}, C_{Q3} \) and \( C_{Q4} \) are much smaller than \( C_{AD} \) and \( C_{BD} \).

\[
\begin{align*}
C_{Q1} &= k_1 v_{Q1} \\
C_{Q3} &= k_1 v_{Q3} \\
C_{Q4} &= k_1 v_{Q4}
\end{align*}
\]

Fig. 12. Extract \( C_{AD} \) and \( C_{BD} \) for a half-bridge LLC resonant converter under working condition.

In Fig. 12, if both the input and the output of the converter are disconnected from the ground, the measured working waveforms for \( v_{AD} \) and \( v_{DB} \) under converter working conditions will be determined by \( nv_{Q1}, C_{AD} \) and \( C_{BD} \). So \( C_{ID} \) and \( C_{BD} \) can still be calculated from (38) with \( v_g \approx nv_{Q1} \).

VI. SIMULATION AND EXPERIMENTAL VERIFICATION

A. Verification with a LLC resonant converter

Experimental verification is first conducted with a 1kW full-bridge LLC resonant converter in Fig. 10 with both input and output ungrounded. The input and output rated voltages are 48V and 12V respectively. The switching frequency is 910kHz. \( C_{AD} \) and \( C_{BD} \) are much larger than other capacitances in the model, so the influence of other capacitances can be ignored in the measurements.

In order to verify the two-capacitor transformer winding capacitance model and the capacitance extraction technique, two measurements are conducted based on the models 2 and 11 in Fig. 4. Fig. 13 (a) is the measured voltage waveforms of \( v_{AD} \) and \( v_{DB} \). The ratio \( h \approx 1.5 \) was calculated from the magnitudes of the voltages. According to (37), the transformer turn ratio is 4:1:1, it is predicted that \( C_{BC}/C_{BE}=v_{EB}/v_{BC} \approx -4.3 \). From the measured voltage magnitudes in Fig. 13 (b), it is shown that the measured results match the predicted very well.

The total capacitance \( k_1 \) can be measured as 4.2nF by shorting the primary terminals and secondary terminals of the transformer shown in Fig. 11(a). \( C_{BD} \) and \( C_{AD} \) are calculated from (38) as 1.68nF and 2.52nF.

By performing a CM EMI noise prediction, the proposed transformer modeling technique can be further verified. The CM spectrum is simulated with the transformer model in Fig 10(c) and the extracted parameters when both input and output are grounded. Noise sources \( v_{Q1}, v_{Q2}, \) and \( v_{Q3} \) used in simulation are directly from the measured voltage waveforms with an oscilloscope. Fig. 14 shows the comparison between the simulated and measured noise spectra. The noise spikes match well especially in low frequency range. The background noise of the measured noise is related to the experiment environment and the spectrum analyzer settings. The simulated background noise is related to the sampling rate and the number of FFT points. These two normally don’t match. However, this does not influence EMI analysis.

As analyzed previously, if \( C_{AD} \) is equal to \( C_{BD} \), the CM noise can be reduced. This is achieved by paralleling a 0.84nF capacitor between A and D in the experiment. A 25dB CM noise reduction is achieved at the switching frequency in the measured EMI in Fig. 15. This verifies the analysis in the paper.
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Fig. 14. Comparison of the simulated and measured CM noise spectra of the LLC resonant converter.

Fig. 15. Comparison of the measured CM noise spectra of the LLC resonant converter before (CM EMI 1) and after (CM EMI 2) CM noise cancellation.

B. Verification with a flyback converter

The 2nd experimental verification is conducted with a 45W AC/DC flyback converter. Its input voltage is 120VAC. Its output voltage is 12VDC. It has a switching frequency 65kHz. A diode bridge is located between the LISNs and the input DC capacitor in Fig. 5(a). The CM noise model is similar to that in Fig. 5(c) except that the LISN’s 25Ω impedance should be replaced with the total impedance of the CM impedance of the diode bridge and the LISN’s 25Ω impedance because they are in series in the CM noise path. The CM impedance of the diode bridge is very small when one or two diodes conduct currents. When all diodes are off, it is determined by the junction capacitance of the diodes so it is big. The condition for CM noise cancellation is therefore still \( C_{BC} = -C_{Q1}. \)

\( C_{AC} \) and \( C_{BC} \) can be measured similarly to that in Fig. 11 except that the secondary has only one winding. The total capacitance \( k_i \) is measured as 110pF by shorting the primary terminals and secondary terminals of the transformer. To extract \( C_{AC} \) and \( C_{BC}, \) a 65kHz, 10V \( p-p \) sinusoidal signal is added to the primary winding with a signal generator having 50Ohm source impedance. The voltages \( v_{AB} \) and \( v_{AC} \) are measured with an oscilloscope. Because the voltage probes of the oscilloscope have capacitance \( C_{probe} = 22pF, \) whose effects on voltage measurement cannot be ignored, when calculating \( C_{AC} \) and \( C_{BC}, \) \( C_{probe} \) must be considered. On the other hand, since \( C_{BC} \) and \( C_{BE} \) are much larger than \( C_{probe} \) in Fig. 13, \( C_{probe} \)’s effect is ignored in Fig. 13.

Fig. 16. Measured \( v_{AB} \) and \( v_{AC} \) of a flyback transformer with a signal generator and an oscilloscope.

Fig. 17. Comparison of the simulated and measured CM noise spectra of the flyback converter.

Fig. 18. Comparison of the measured CM noise spectra of the flyback converter before (CM EMI 1) and after (CM EMI 2) CM noise cancellation.

To verify the proposed transformer model, CM noise prediction and reduction were conducted for the flyback converter. The CM spectrum is simulated with the transformer model in Fig. 5(c) and the extracted parameters when both input and output are grounded. Noise source \( v_{Q1} \) used in the simulation are directly from the measured voltage waveforms with an oscilloscope. In Fig. 17, a simulated CM noise spectrum is compared with the measured one. The two
matches quite well in general. The mismatch above 6MHz is due to other high frequency parasitic parameters which is not modeled in Fig. 5(c) in the CM noise loop.

Since $C_{QI}=0$, the 9.5pF $C_{BC}$ should be canceled to cancel CM noise. This can be achieved by adding a capacitor between D and A to generate a reverse CM current to cancel the CM noise from B to C. Because the turns ratio $n=5$, a 47pF capacitor is used for cancellation.

The measured CM EMI noise spectra before and after adding the compensation capacitor are shown in Fig. 18. It is shown that after the compensation, a maximum 18dB noise reduction is achieved from 150kHz to above 10MHz, which verifies the effectiveness of the proposed modeling and noise reduction techniques.

VII. CONCLUSIONS

This paper proposes a transformer winding capacitance modeling technique for the CM EMI analysis in isolated power converters. The developed modeling technique has multiple benefits: 1) it is derived based on general conditions thus it has a wide range of applications for CM noise analysis and cancellation; 2) the lumped capacitances of the model can be obtained by simple measurements; 3) the model has great flexibility in simplifying the CM EMI circuit model. The developed technique was validated with both simulations and experiments.

With the help of the proposed model, researchers and engineers can free themselves from the examination of transformer physical structures when analyze the CM EMI performance of isolated converters. As long as the conditions defined in the paper are met, the developed two-capacitor model can always be applied to the transformer modeling for CM noise analysis. The proposed lumped capacitance extraction technique for the developed model is not only easy to use, but also able to evaluate transformer’s CM characteristics in many applications. Designers can easily make a balanced transformer with the proposed capacitance extraction technique.

REFERENCES

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