A 0.65-to-10.5 Gb/s Reference-Less CDR With Asynchronous Baud-Rate Sampling for Frequency Acquisition and Adaptive Equalization

Seungham Choi, Hyunwoo Son, Jongshin Shin, Sang-Hyun Lee, Byungsub Kim, Member, IEEE, Hong-June Park, Senior Member, IEEE, and Jae-Yoon Sim, Senior Member, IEEE

Abstract—This paper presents a continuous-rate reference-less clock and data recovery (CDR) circuit with an asynchronous baud-rate sampling for frequency acquisition and results in a fast coarse lock process. The CDR guarantees a robust operation of a fine locking even in the presence of large input data jitter due to the adaptive equalization and a jitter-tolerable rotational frequency detector (RFD) that eliminates a dead-zone problem with a simple circuitry. The fabricated CDR in 65 nm CMOS shows a wide lock range of 0.65-to-10.5 Gb/s at a bit error rate (BER) of $10^{-12}$. The CDR consumes 26 mW from a single supply voltage of 1 V at 10 Gb/s including the power consumption for equalizer. By an adaptive current bias control, the power consumption is also linearly scaled down with the data rate, exhibiting a slope of about 2 mW decrease per Gb/s.

Index Terms—Adaptive equalization, asynchronous sampling, clock and data recovery (CDR), continuous time linear equalizer (CTLE), frequency acquisition, reference-less CDR, rotational frequency detector (RFD).

I. INTRODUCTION

In modern communication systems, clock and data recovery (CDR) circuits are widely used as a core block at the receiver side for sampling and retiming the incoming data by recovering clock timing information. The CDR using an external reference clock operates at the pre-defined data rate so that it limits flexibility to meet various applications. To cover a wide range of bit rate, there exist two kinds of architectures: multi-rate CDR [1], [2] and continuous-rate CDR [3]–[7]. The multi-rate CDR can acquire the timing information using multiple reference clocks [1] or single reference clock with a programmable divider [2]. Nevertheless, multi-rate CDRs only operate at several pre-defined data rates. To continuously cover a wide operation range, the continuous-rate CDR has been researched.

The design of continuous-rate reference-less CDR has presented challenges for wide-range frequency acquisition, low-power consumption with scalability along with the data rate, and fast frequency lock. Although the previously reported architectures [3]–[7] achieved the continuous-rate operation, they still have several drawbacks in achieving all of such requirements. The coarse/fine frequency acquisition scheme [3] has been the first approach for a wide-range reference-less CDR. However, this architecture suffers from non-scalable power dissipation to the data rate since an LC voltage controlled oscillator (VCO) followed by a frequency divider still operates at high frequency even for very low data rate recovery. To achieve the scalability in power consumption along with the data rate, a wide-range CMOS VCO has been taken in continuous-rate reference-less CDRs [4]–[6]. Although the delay locked loop (DLL) based approach [4] also covers a wide range of bit rates with the coarse/fine delay tracking, there is a stringent matching requirement between a voltage controlled delay line (VCDL) and a VCO and it requires large power consumption on high-speed buffers. The stochastic sub-harmonic frequency extraction [5] efficiently extracts the data rate by counting input data transitions. However, it generates very low frequency for the frequency reference and also assumes a pre-defined input transition density for frequency acquisition. A bang-bang phase detector (PD) output counting [6] and offset-controlled asymmetric linear PD [7] have been recently proposed for the continuous-rate operation with a simple digital logic. They should perform a linear search so that searching algorithms scan whole frequency range from the minimum or maximum until they find out the target. When used with a wide frequency range, repeating the frequency comparison with every change of 1b VCO resolution eventually limits the fast frequency detection. There has been no reference-less CDR achieving all the requirements of wide-range and fast frequency acquisition with low power consumption scalable to the data rate.

This paper presents a reference-less CDR with an asynchronous baud-rate sampling scheme which achieves all of such requirements and an adaptive equalization [8], [9] at the same time. It also introduces a new jitter-tolerable rotational frequency detector that eliminates a dead-zone problem in the presence of input data jitter with a simple circuitry. Section II
describes the concept of the proposed scheme, and Section III describes the circuit implementation in detail. Section IV presents the stochastic analysis of the proposed frequency acquisition scheme. Section V summarizes the measurement results, and Section VI concludes this work.

II. FREQUENCY LOCK WITH ADAPTIVE EQUALIZATION

A. Asynchronous Sampling

Fig. 1(a) shows the core circuit for the proposed asynchronous baud-rate sampling formed with a D flip-flop for input sampling and two counters (CNTs), where one counts the number (N_{Di}) of rising transitions in the input data (Di) while the other counts the number (N_{Do}) of rising transitions in the sampled data (Do). For the D flip-flop, we adopted a typical sense-amp type circuit since it receives a CMOS level signal generated by an equalizer followed by a CML-to-CMOS converter which will be described in the next subsection. N_{Do}/N_{Di} versus the ratio between clock frequency (f_{CLK}) and data rate (D.R) is characterized with simulations for various channel loss [Fig. 1(b)]. If the sampling clock frequency (f_{CLK}) is higher than or equal to the data rate when there is no channel loss [Fig. 2(a)], Do contains all the transition events of Di. Therefore, N_{Do} equals N_{Di}. On the other hand, if f_{CLK} is lower than the data rate [Fig. 2(b)], the undersampled result would miss some input transition information, resulting in smaller N_{Do} than N_{Di}. Therefore, the difference between f_{CLK} and the data rate can be estimated by comparing N_{Di} and N_{Do}. This missed transition occurs more frequently as the sampler receives isolated 1-UI pulse. If the input to the sampler experiences a lossy channel, the systematic jitter occurs by the inter-symbol interference (ISI). Since the ISI-induced jitter makes the isolated 1-UI pulse even shorter, the sampled data (Do) contains a smaller number of transitions. By utilizing this relation, the asynchronous sampling can be also applied to an adaptive equalization as well as the data rate acquisition.

B. Adaptive Equalization and Frequency Acquisition

Fig. 3(a) illustrates the detailed control loop for generation of a sampling clock (CLK) by a digitally controlled oscillator (DCO). In this work, two 9b counters are used for N_{Do} and N_{Di}, and the loop also contains a comparator (COMP) which checks whether N_{Do} is lower than N_{Di} or not, when N_{Di} reaches 511. According to the comparison result, the comparator drives its output (UP/DN) to a successive approximation register (SAR) that performs a binary search of the 10b DCO code (DCO[9:0]). By the transfer characteristic of N_{Do}/N_{Di} [Fig. 1(b)] with 0-dB loss, the asynchronous sampling clock from the DCO becomes eventually locked to the baud-rate after the completion of the binary search. However, as shown in Fig. 1(b) with some channel loss, the exact baud-rate frequency can miss transition events if the input data contains ISI-induced jitter. In this case, the DCO would be locked to a higher frequency than the baud-rate to count all the transition events.

This work employs a continuous-time linear equalizer (CTLE) to compensate the channel loss, hence minimizing the ISI-induced jitter. The CTLE was designed to control the equalizing gain using a 3b CTLE gain code (G[2:0]). To find the optimal CTLE gain, the binary search of DCO[9:0] by the SAR is repeated as G[2:0] is forced to change from 000 to 111. During this linear scan process for G[2:0], where each step is composed of the binary search for DCO[9:0], a register (R_D) stores the G[2:0] whenever the SAR finds a new minimum DCO[9:0]. The new minimum DCO[9:0] is also stored in a register (R_C). Since both of the under-equalization and over-equalization increase ISI-induced jitter, obtaining the minimum DCO[9:0] at a given G[2:0] whenever the SAR finds a new minimum DCO[9:0]. The new minimum DCO[9:0] is also stored in a register (R_D). Since both of the under-equalization and over-equalization increase ISI-induced jitter, obtaining the minimum DCO[9:0] at a given G[2:0] can be interpreted as the ISI-induced jitter is eventually minimized by the optimal CTLE gain. Therefore, the minimum DCO[9:0] with a given G[2:0]
leads to the data rate acquisition with adaptive equalization [Fig. 3(b)]. To achieve the power consumption scaled along with the data rate [9], the CTLE bias code (C[3:0]) is also adaptively controlled to flow proportional DC current to the data rate. C[3:0] of the current step is simply set to 4 MSBs of DCO code obtained after the completion of the previous linear search step. Similarly to G[2:0], a register (R_C) stores the C[3:0] whenever the SAR finds a new minimum DCO[9:0]. Before the linear search, one extra 10b binary search is inserted in the beginning with forcing G[2:0] to 000 and C[3:0] to 1111. It roughly obtains a reasonable C[3:0] for CTLE bias current to start the first step in the linear search. At the end of the linear search, G[2:0], C[3:0], and DCO[9:0] are respectively replaced with R_G, R_C, and R_D, as a result of the adaptive equalization with the data rate detection.

Data edge counting schemes have been often taken for the data rate acquisition [5] or the adaptive equalization [9]. To extract the data rate information, the stochastic sub-harmonic frequency extraction [5] counts the clock edges within a timing window given by the number of data edges. On the other hand, our scheme counts the sampled data edges within a timing window given by the number of data edges. Since the number of sampled data edges is much more sensitive to the channel loss than the number of data edges itself, the sampled data edge counting can uniquely achieve both the data rate detection and the adaptive equalization. Previous work on the adaptive equalization with the data edge counting [9] can be simply understood by switching the roles of the clock edges and the data edges in [5]. The number of data edges in [9] would not change once CTLE gain exceeds the minimum that starts to detect all the data transitions. On the other hand, the counted number of sampled data edges sensitively reflects the amount of jitter caused by both under- and over-equalizations, showing a higher distinguishability for finding the optimal value in the adaptive equalization.

It can be also noted that this adaptive equalization maximizes horizontal window rather than the vertical window of the data eye. Maximizing the horizontal sampling window is more beneficial in reducing the bit error rate (BER) since chances of failure in small voltage detection by metastability become further reduced in the sampler operation with scaled CMOS technology.

III. CIRCUIT IMPLEMENTATION

Fig. 4 shows an overall circuit diagram of the CDR. For a wide-range operation, this work employs a coarse/fine 2-step frequency acquisition scheme [3], [4]. The proposed baud-rate asynchronous sampling scheme does not require any extra clock source but uses the oscillator in CDR loop. The frequency acquisition and adaptive equalization complete the coarse lock. During coarse lock period, the loop filter (LF) stays at VDD/2 with charge pumps (CPs) disabled. When the coarse lock ends, the CDR with a dual-loop architecture whose loops are merged in a single LF [10], [11] takes over the loop control and performs the fine phase and frequency lock with a conventional full-rate binary PD [12] and a modified rotational frequency detector (RFD) which guarantees a robust lock operation even in the presence of input data jitter.

A. Adaptive Equalizer

To adapt the channel loss, a 3-stage CTLE [8], [9], [13] is adopted. The CTLE [Fig. 5(a)] features a degenerative structure with a source resistor (R_S) and a capacitor (C_S) generating additional zero (ω_z) and pole (ω_p1), leading to a transfer function of the CTLE as

\[ T(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{g_m R_L}{1 + \frac{g_m R_C}{2}} \cdot \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p1}} \cdot \frac{1 + \frac{s}{\omega_p2}}{1 + \frac{s}{\omega_p}} \]

where \( \omega_{p1} = (1 + g_m R_S/2)/(R_S C_S) \), \( \omega_{p2} = 1/(R_L C_L) \), \( \omega_Z = 1/(R_S C_S) \) and \( g_m \) is the transconductance of the input transistor. Since C[3:0] is closely related to the data rate, it is used to control the bias current (I_BIAS) and the load resistor (R_L) to adjust the bandwidth and the common-mode level of the output. The common-mode level is controlled by only two MSBs, C[3:2], since it does not seriously affect the overall CTLE performance. G[2:0] controls the R_S to adjust the low frequency gain. Fig. 5(b) and (c) are simulated AC responses of the 3-stage CTLE when C[3:0] is 0000 and 1111, respectively. Fig. 5(d) summarizes the average resolution of the gain boosting as C[3:0] changes for voltage and temperature corners. The 3-stage CTLE is followed by a fully differential CML-to-CMOS converter (C-to-C). The C-to-C consists of an OTA stage and multiple cross-coupled inverter stages that ensure CMOS-level swing with half-VDD common mode voltage and preserve the transition timing of input data.

B. Jitter-Tolerable RFD

The Potbacker RFD [14] is conventionally used frequency detector based on the quadricorrelator [15], [16] realized with digital circuits. As shown in Fig. 6(a), the conventional RFD can detect the frequency error with the low circuit complexity. However, it suffers from a dead-zone in the presence of input data jitter. Fig. 6(b) and (c) respectively describe the state diagrams (Q1, Q2) which generate wrong decisions under jittery condition when f_{CLK} < data rate (UP state) and
Fig. 5. (a) CTLE circuit. (b) AC response with $C[3:0] = 0000$ and (c) with $C[3:0] = 1111$. (d) Average resolution of gain boosting according to $C[3:0]$. 

$f_{CLK} >$ data rate (DN state). There are four states according to combinations of $(Q1, Q2)$. The rotating direction indicates the sign of the frequency difference. ISI-induced jitter in the input data ($D_{IN}$) causes an instantaneous change in the data rate. Therefore, it can make the states rotate to wrong direction for a short period of time at the boundaries. Since RFD outputs ($UP_{Conv}$ and $DN_{Conv}$) are updated with opposite polarity only at the rising transition of $Q2$, an unwanted glitch-like rising transition of $Q2$ due to the input data jitter causes a wrong output to be held for significantly long time. This error occurs more frequently as the amount of jitter increases, resulting in a large dead-zone.

To address the dead-zone problem in the RFD, a modified digital quadricorrelator frequency detector (M-DQFD) was introduced in [17], where complicated logic blocks are required to find out if the frequency error exists in the dead-zone. In addition, multiple case-by-case frequency-error indicators are needed for right frequency detection. In this paper, we propose a new dead-zone eliminated RFD with only a few gates added to the conventional RFD [Fig. 7(a)]. The proposed RFD achieves not only improvement of the input-jitter tolerability with a single frequency-error indicator but self-disabling [11] when locked. As shown in Fig. 7(b) and (c), the RFD has a valid and an invalid region for the output according to $Q2$. When $Q2$ is high, $UP_x$ and $DN_x$ are blocked so that both of RFD outputs ($UP_{Prop}$ and $DN_{Prop}$) become low. Only when $Q2$ is low, the output becomes valid. Similarly to the conventional RFD, the error occurs at an unwanted falling transition of $Q2$. However, the state will recover the correct direction after a short wandering due to the phase accumulation of the frequency difference. In other words, the state eventually enters invalid region after generating the wrong decision. Therefore, the wrong decision cannot affect the loop. On the other hand, the state enters valid...

Fig. 6. (a) Conventional RFD. (b) State diagram and error occurrence at $f_{CLK} <$ data rate (UP state). (c) State diagram and error occurrence at $f_{CLK} >$ data rate (DN state).
When the loop is locked, the state falls on II or III [Fig. 7(d)], where Q2 stays at high. It blocks RFD output and prevents the RFD from disturbing the phase-locked VCO. Therefore, this tri-state operation automatically deactivates the RFD near lock state and reactivates it whenever the loop loses the lock without an additional switching. It should be noted that the self-disabling of the RFD also helps achieving a large bandwidth for frequency lock. Although the proposed scheme reduces the gain of the RFD by half, the CP driving strength with the RFD can be set to much larger than that with the conventional RFD. As a result, the larger bandwidth with the self-disabling enables a quick adjustment of a little frequency offset after the coarse lock and achieves better jitter performance at the fine-locked phase.

Fig. 8(a) compares simulated outputs of the conventional RFD and the proposed RFD in the presence of input data jitter. 10-Gb/s lossy data and 9.9-GHz clock (UP state) are applied to both RFDs. While outputs (UP_{Conv} and DN_{Conv}) of the conventional RFD suffer from false decisions causing a serious dead-zone, the outputs (UP_{Prop} and DN_{Prop}) of the proposed RFD reduce the effect of false decisions to very short pulses which have negligible impact on correct operation [Fig. 8(b)].

C. Clock Generation

The CDR employs a supply-regulated inverter-based oscillator [18] whose unit cell is described in Fig. 9(a). The VCO generates a 4-phase full-rate CLK, and its supply voltage (VDDVCO) is provided by the VCTRL generator (VCTRL Gen.) followed by a regulator (REG) [Fig. 9(b)]. The VCTRL Gen. consists of a 10b binary current-mode DAC (I-DAC) to reflect the coarse-locked DCO[9:0] and a tri-state inverter-based variable gain amplifier (VGA) whose input is a LF output (VPL). As shown in Fig. 10(a), I-DAC enables a wide and linear range of the DCO frequency (f_{CLK}). The gain of the VGA is adjusted by 2MSBs of DCO code which adaptively controls the loop bandwidth for a wide frequency range operation. Fig. 10(b) is the simulated VCTRL versus VPL at the middle of
an each band defined by 2 MSBs of DCO code. The resulting oscillator gain (KVCO) in the fine locking process is given by

\[ KVCO = f_{CLK} \times VPL = \left( \frac{f_{CLK}}{VCTRL} \right) \times \left( \frac{VCTRL}{VPL} \right). \]  

(2)

It is 1.0 GHz/V, 2.5 GHz/V, 4.5 GHz/V, and 7.0 GHz/V when the 2 MSBs of DCO code are 00, 01, 10, and 11, respectively.

A level shifter (LS) converts the VCO output to a balanced CMOS-level output.

IV. STOCHASTIC ANALYSIS

This section examines the proposed frequency acquisition scheme with the stochastic analysis. For simplicity to get an insight, a random input stream with a transition density of 1/2 is assumed to be applied through an ideal channel without ISI-induced jitter.

A. Full-Rate Operation

As explained in Section II, if VCO frequency \( f_{CLK} \) is higher than or equal to the data rate, the input sampler in the asynchronous sampling core [Fig. 1(a)] detects all the transition events of \( D_i \), which leads to \( \frac{N_{Do}}{N_{Di}} = 1 \). On the other hand, in case of the undersampling where \( f_{CLK} \) is lower than the data rate, the input sampler would miss some input transitions, resulting in less \( N_{Do} \) than \( N_{Di} \). Assuming \( N_{Di} \) and \( N_{Do} \) are counted for a given time \( T_{Monitor} \) in case of the undersampling as in Fig. 11, they eventually approach theoretical values as

\[ N_{Di} = \frac{T_{Monitor}}{1/4}, \quad f_{CLK} \geq D.R \]  

\[ N_{Di} = \frac{T_{Monitor}}{1/4}, \quad f_{CLK} < D.R \]  

(3.a)\( (3.b)\)

where \( T_{CLK} \) is the clock period and the factor of 1/4 reflects the probability of the rising transition which only contributes to \( N_{Do} \) and \( N_{Di} \). From (3.a) and (3.b), \( N_{Do}/N_{Di} \) along with \( f_{CLK}/D.R \) becomes

\[ \frac{N_{Do}}{N_{Di}} = \frac{1}{f_{CLK}/D.R} \]  

(3.c)

This reveals that \( N_{Do}/N_{Di} \) is linearly proportional to the ratio between \( f_{CLK} \) and the data rate. Consequently, \( N_{Do}/N_{Di} \) along with \( f_{CLK}/D.R \) becomes

\[ \frac{N_{Do}}{N_{Di}} = \begin{cases} 1, & \text{for } f_{CLK} \geq D.R \\ \frac{1}{f_{CLK}/D.R}, & \text{for } f_{CLK} < D.R \end{cases} \]  

(4)

which verifies the RTL-level simulation result [Fig. 1(b)] with 0-dB loss.

B. Detection Time and Accuracy

When the VCO frequency is higher than the data rate, every transition is detected by the oversampling. Therefore, this subsection focuses on the undersampling which experiences the miss of transition events, and hence makes a difference between \( N_{Di} \) and \( N_{Do} \). As the difference in \( N_{Di} \) and \( N_{Do} \) is proportional to \( T_{Monitor} \), a longer \( T_{Monitor} \) helps to get statistically more accurate result, especially when the frequency difference is small. Thus, there is a trade-off between the detection time and the accuracy.

<table>
<thead>
<tr>
<th>Data rate</th>
<th>1 Gbs</th>
<th>5 Gbs</th>
<th>10 Gbs</th>
</tr>
</thead>
<tbody>
<tr>
<td># of bits ( (N_{Di}) )</td>
<td>( f_{CLK} ) [GHz]</td>
<td>( T_{Monitor} ) [nsec]</td>
<td>( f_{CLK} ) [GHz]</td>
</tr>
<tr>
<td>7 (128)</td>
<td>0.992</td>
<td>512</td>
<td>4.961</td>
</tr>
<tr>
<td>8 (256)</td>
<td>0.996</td>
<td>1024</td>
<td>4.980</td>
</tr>
<tr>
<td>9 (512)</td>
<td>0.998</td>
<td>2048</td>
<td>4.990</td>
</tr>
<tr>
<td>10 (1024)</td>
<td>0.999</td>
<td>4096</td>
<td>4.995</td>
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* Error [ppm] = \( (f_{CLK} - D.R)/D.R \times 10^6 \)
According to (3.a), each 1-bit comparison cycle \( T_{\text{Monitor}} \) during the binary search is expressed as

\[
T_{\text{Monitor}} = N_{\text{Di}} \cdot \frac{1}{4} \cdot \left( 1 - U_I \right) = \frac{2 \cdot \# \text{ of Counter bits}}{D.R}. \tag{5}
\]

The maximum detectable clock frequency \( \dot{f}_{\text{CLK.UP}} \) which can be detected to be “lower” than the data rate is obtained by replacing \( N_{\text{Do}} \) with \( N_{\text{Di}} - 1 \) in (3.c), representing one missing event, as

\[
\frac{N_{\text{Di}} - 1}{N_{\text{Di}}} = \frac{\dot{f}_{\text{CLK.UP}}}{D.R} \tag{6.a}
\]

or

\[
\dot{f}_{\text{CLK.UP}} = D.R - \frac{D.R}{2 \cdot \# \text{ of Counter bits}}. \tag{6.b}
\]

Both of (5) and (6.b) include the number of counter bits as a variable, indicating the trade-off between the detection time and the detection resolution. Table I summarizes \( T_{\text{Monitor}} \) and \( \dot{f}_{\text{CLK.UP}} \) for various cases of the numbers of counter bits and the data rates. In this work, 9-bit counting is selected as a compromise of the detection time and the coarse-lock accuracy.

The frequency error after the coarse lock is small enough and can be safely handled by the proposed RFD even in the presence of ISI-induced jitter.

V. MEASUREMENT RESULTS

The proposed circuit is fabricated in 65 nm CMOS process. Fig. 12(a) shows a micrograph of the die whose active area is 0.21 mm\(^2\) including input/output buffers for test. In the testing setup [Fig. 12(b)], a full-rate PRBS data provided by the BER tester (J-BERT) is applied to the chip through FR4 traces with different lengths. For the channel characterization, we measured the transmission-line-only characteristics and added the effect of the parasitic with an inductance of 1 nH and a capacitance of 1.5 pF for modeling SMA, 2 cm-long PCB trace from SMA to die, wire bonding, and pad [Fig. 12(c)]. The recovered clock is monitored with half-rate for relieving the bandwidth constraints of the output buffers.

Fig. 13 demonstrates the measured trace of the clock frequency \( f_{\text{CLK}} \) during whole locking process at 4 Gb/s with a 40 cm PCB channel (about 5 dB loss). The graph clearly shows nine 10b SAR steps which consist of one step for the CTLE initialization and eight steps for the CTLE gain.
linear search. At the beginning of each step, $f_{CLK}$ is reset to the center frequency of the DCO where DCO[9:0] is set to “1000000000” for starting the binary search. The initialization step is to obtain a reasonable C[3:0] to start the first step of the linear search and following eight steps eventually find the optimum CTLE gain with the data rate acquisition. Each steps is completed in $2^{\#}$ of Counter bits × (1/rising transition density of random data) × \# of DCO bits, or only 20,480 UI (5.12 $\mu$s at 4 Gb/s and 1.95 $\mu$s at 10.5 Gb/s) in this design. The completion of the total nine steps requires about 184,320 UI (46.1 $\mu$s at 4 Gb/s and 17.6 $\mu$s at 10.5 Gb/s).

At the end of the linear search, $f_{CLK}$ is replaced to $f_{CLK_{min}}$ which is provided by the stored minimum DCO[9:0]. G[2:0] and C[3:0] are also replaced with the stored values that makes the minimum DCO[9:0]. Imperfectness of sampler such as metastability and sensitivity-induced error might miss signal transition. It causes the coarse-locked $f_{CLK_{min}}$ to be slightly higher than the target. After the coarse lock, fine lock process takes over the loop control with the jitter-tolerable RFD and the PD.

To verify if the proposed scheme finds the optimum, the coarse-locked $f_{CLK}$ by the proposed scheme is compared with the coarse-locked $f_{CLK}$ with a manually given CTLE gain. As the gain code, G[2:0], changes from 000 to 111, the minimum $f_{CLK}$ and the minimum BER are achieved at the same gain codes [Fig. 14]. 20 cm- and 40 cm-long traces on PCB are used as channels for 9 Gb/s and 8 Gb/s $2^{15} - 1$ PRBS patterns, respectively, presenting 11 dB and 14 dB losses at each Nyquist frequency including the effect of the parasitic. The proposed adaptive equalization scheme successfully finds out the optimum CTLE gain.

Jitter histograms of the recovered clock were monitored with half-rate at 0.65 Gb/s [Fig. 15(a)] and at 10.5 Gb/s [Fig. 15(b)]. The rms jitters of both cases are 38.5 ps and 3.4 ps, respectively. Fig. 15(c) shows measured phase noise of the recovered clock (after divided by 2) with a data rate of 10.5 Gb/s. Fig. 15(d) illustrates the jitter tolerance at 10 Gb/s, using $2^{15} - 1$ PRBS input with a BER criterion of $10^{-12}$. 
The proposed CDR consumes 26 mW from a supply voltage of 1 V at 10 Gb/s including the equalizer power consumption. As shown in Fig. 16(a), the total power consumption is linearly scaled down along with the data rate except for an offset of 5 mW for the minimum bias current for analog circuits (CTLE, C-to-C, CP, REG, and VCTRL Gen.). The CTLE bias is also adaptively controlled to flow proportional DC current to the data rate [Fig. 16(b)]. Table II compares the performance with previously reported state-of-the-art reference-less CDRs.

### VI. Conclusion

A 0.65-to-10.5 Gb/s continuous-rate reference-less CDR has been implemented in 65 nm CMOS technology. The proposed asynchronous sampling makes it possible to adopt a SAR-based frequency tracking, hence enabling a fast frequency acquisition. In addition, an adaptive equalization is also achieved by a linear search while repeating the same frequency acquisition process. The fabricated CDR shows a wide lock range of 0.65-to-10.5 Gb/s at a BER of $10^{-12}$. The CDR consumes 26 mW at 10 Gb/s, and the power consumption is scaled down along with the data rate.

### APPENDIX

Though this work used the full-rate clocking for data recovery, the sub-rate operation [4]–[6], [10], [19] can be also considered to relieve the speed requirements of the sampler and clock buffers. This section investigates how the proposed frequency acquisition scheme can be used with a sub-rate clocking.

The frequency acquisition with a sub-rate clock can be considered by inserting a frequency divider at the frontend of the transition detection core [Fig. 17(a)]. The division factor of 1 ($n = 1$), 2 ($n = 2$), and 4 ($n = 4$) are used with the full-rate, the half-rate, and the quarter-rate clocks, respectively. RTL-level simulation [Fig. 17(b)] of $N_{D_0}/N_{D_{1,n}}$ reveals that it can still distinguish the boundary between $f_{CLK} \geq D.R_n$ and $f_{CLK} < D.R_n$, where $D.R_n$ is defined as

$$D.R_n = \frac{1}{\text{Minimum pulse duration in } D_{i,n}} = \frac{1}{n \cdot U.T} \tag{7}$$

The transfer curve which would be a straight line with the full-rate is shifted up and curved at the sub-rate. The shifted amount

### Table II: Performance Summary and Comparison

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</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>65 nm</td>
<td>0.13 µm</td>
<td>65 nm</td>
<td>0.18 µm</td>
<td>65 nm</td>
</tr>
<tr>
<td>Supply [V]</td>
<td>1.2</td>
<td>1.2</td>
<td>1.2/1.0</td>
<td>1.8</td>
<td>1.0</td>
</tr>
<tr>
<td>Data rate [Gb/s]</td>
<td>0.65–8</td>
<td>0.5–2.5</td>
<td>4–10.5</td>
<td>8.2–10.3</td>
<td>0.65–10.5</td>
</tr>
<tr>
<td>Architecture</td>
<td>Quarter-rate</td>
<td>Half-rate</td>
<td>Half-rate</td>
<td>Full-rate</td>
<td>Full-rate</td>
</tr>
<tr>
<td>Acquisition</td>
<td>Reference-less</td>
<td>Reference-less</td>
<td>Reference-less</td>
<td>Reference-less</td>
<td>Reference-less</td>
</tr>
<tr>
<td>Equalization</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Oscillator</td>
<td>Ring</td>
<td>Ring</td>
<td>Ring</td>
<td>LC</td>
<td>Ring</td>
</tr>
<tr>
<td>Jitter [P_{err}/P_{j}]</td>
<td>@8Gb/s</td>
<td>@2Gb/s</td>
<td>@10Gb/s</td>
<td>0.34/7.7</td>
<td>3.4/23.5</td>
</tr>
<tr>
<td>Power [mW]</td>
<td>88.6</td>
<td>6.1</td>
<td>22.5</td>
<td>174</td>
<td>18.7</td>
</tr>
<tr>
<td>FoM [mW/Gb/s]</td>
<td>11.1</td>
<td>3.05</td>
<td>2.25</td>
<td>16.9</td>
<td>1.87</td>
</tr>
<tr>
<td>Area [mm²]</td>
<td>0.11</td>
<td>0.36</td>
<td>1.63</td>
<td>0.54</td>
<td>0.21</td>
</tr>
</tbody>
</table>

* Random jitter / pattern-dependent deterministic jitter at recovered data

* *1 mW for 3-stage CTLE and 1.2 mW for CML-to-CMOS converter at 10 Gb/s

---

**Fig. 17.** Sub-rate operation. (a) Circuit. (b) Transfer characteristic of frequency detection.
TABLE III
STOCHASTIC ANALYSIS OF SUB-RATE OPERATION

<table>
<thead>
<tr>
<th></th>
<th>Full-Rate (n=1)</th>
<th>Half-Rate (n=2)</th>
<th>Quarter-Rate (n=4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ρ[i]</td>
<td>1/2^i</td>
<td>1/2^i</td>
<td>1/2^i</td>
</tr>
<tr>
<td>T[n]</td>
<td>1-UI</td>
<td>2-UI, 3-UI</td>
<td>4-UI, 5-UI, 6-UI, 7-UI</td>
</tr>
<tr>
<td>ρ[n]</td>
<td>1/2^n</td>
<td>1/2^n</td>
<td>1/2^n</td>
</tr>
<tr>
<td>1/(T[n]i)/(T[n]i)</td>
<td>1.00</td>
<td>1.00, 0.67</td>
<td>1.00, 0.80, 0.67, 0.57</td>
</tr>
</tbody>
</table>

Table III: Stochastic Analysis of Sub-Rate Operation

Fig. 18. Occurrence density of n-UI pulse in Di_n.

random bit stream, ρ[1], ρ[2], and ρ[4] respectively become 1/2^2, 1/2^3, and 1/2^4. Note that T_n[i] and ρ[n] represent the pulse duration and the corresponding occurrence density of the isolated minimum-UI pulse in Di_n.

The input sampler in Fig. 17(a) can clearly sample the pulses whose duration is longer than or equal to clock period (T_CLK) and stochastically misses the pulses whose duration is shorter than T_CLK. With the clock period range of T_n[i] < T_CLK ≤ T_n[i+1], the pulses whose duration is between the minimum (T_n[n]) and T_n[i] can be either sampled or missed depending on the clock phase. Therefore, through the asynchronous sampling, the probability (P_Miss[i]) of missing the given i-UI pulse whose duration is shorter than T_CLK is derived as

\[ P_{Miss,i} = \frac{T_{CLK} - T_n[i]}{T_{CLK}} = 1 - \frac{T_n[i]}{T_{CLK}} \]  

(9)

Since the miss of a rising transition occurs by the miss of a pulse through the asynchronous sampling, N_{Do}/N_{Di,n} is described as (10.a), shown at the bottom of the page, or

\[ \frac{N_{Do}}{N_{Di,n}} = \frac{\rho_{e}[n] - (\Sigma_i (1 - T_n[i]/T_{CLK}) \cdot \rho_{n}[i])}{\rho_{n}[n]} \]  

(10.b)

for all i’s satisfying that T_n[i] < T_CLK.
increasing the number of counter bits. Therefore, the proposed
can be easily overcome at the cost of longer detection time by
characteristic at both full-rate and sub-rate operation.

According to (10.b), 

\[
N_{Do} / N_{Di,1} = \begin{cases} 
1 & \text{for } T_{CL} \leq T_{1}, \\
\frac{1}{\rho_{[1]}}(1 - T_{1} / T_{CLK}) & \text{for } T_{1} < T_{CLK} \leq T_{1}[2] 
\end{cases}
\]  

(11.a)
or

\[
N_{Do} / N_{Di,1} = \begin{cases} 
1 & \text{for } T_{CL} \leq T_{1}[1], \\
\frac{T_{1}[1]}{T_{CLK}} & \text{for } T_{1}[1] < T_{CLK} \leq T_{1}[2] 
\end{cases}
\]  

(11.b)

and it is a time-domain interpretation of (4). With the same
approach, \(N_{Do} / N_{Di,2}\) and \(N_{Do} / N_{Di,4}\) are also respectively estimated as

\[
N_{Do} / N_{Di,2} = \begin{cases} 
1 & \text{for } T_{CL} \leq T_{2}[2], \\
\frac{1}{\rho_{[2]}}(1 - T_{2}[2] / T_{CLK}) & \text{for } T_{2}[2] < T_{CLK} \leq T_{2}[3] \\
\frac{1}{\rho_{[2]}}(1 - T_{2}[3] / T_{CLK}) & \text{for } T_{2}[3] < T_{CLK} \leq T_{2}[4] 
\end{cases}
\]  

(12)

and

\[
N_{Do} / N_{Di,4} = \begin{cases} 
1 & \text{for } T_{CL} \leq T_{4}[4], \\
\frac{1}{\rho_{[4]}}(1 - T_{4}[4] / T_{CLK}) & \text{for } T_{4}[4] < T_{CLK} \leq T_{4}[5] \\
\frac{1}{\rho_{[4]}}(1 - T_{4}[5] / T_{CLK}) & \text{for } T_{4}[5] < T_{CLK} \leq T_{4}[6] \\
\frac{1}{\rho_{[4]}}(1 - T_{4}[6] / T_{CLK}) & \text{for } T_{4}[6] < T_{CLK} \leq T_{4}[7] \\
\frac{1}{\rho_{[4]}}(1 - T_{4}[7] / T_{CLK}) & \text{for } T_{4}[7] < T_{CLK} \leq T_{4}[8] 
\end{cases}
\]  

(13)

Fig. 19 shows both simulated and estimated \(N_{Do} / N_{Di,n}\)
versus \(f_{CLK} / D.R_{n}\). In this figure, \(f_{CLK} = 1 / T_{CLK}\) and \(D.R_{n} = 1 / T_{n}[n]\) are used for the frequency-domain representation. It verifies that (10.b) precisely explains the frequency detection characteristic at both full-rate and sub-rate operation.

Although the sub-rate operation suffers from the lower
detection sensitivity as shown by both simulation and analysis, it
can be easily overcome at the cost of longer detection time by
increasing the number of counter bits. Therefore, the proposed

frequency detection scheme can be also applicable to sub-rate
CDRs as well as full-rate CDRs.

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Seunghun Choi received the B.S. degree in Elec-
tronic and Electrical Engineering from Pohang Uni-
versity of Science and Technology (POSTECH),
Korea, in 2011, where he is currently working toward
the Ph.D. degree. His research interests include data converters and
high-speed links.
Hyunwoo Son received the B.S. degree in Electrical Engineering from Pohang University of Science and Technology (POSTECH), Korea, in 2012, where he is currently pursuing the Ph.D. degree.

His research interests include sensor interface circuit, delta-sigma ADC, and neuromorphic circuit.

Jongshin Shin received the B.S., M.S., and Ph.D. degree in electronic and electrical engineering from Seoul National University, Seoul, Korea, in 1997, 1999, and 2004, respectively.

He joined Samsung Electronics, Hwasung, Korea, in 2004 as a Member of Technical Staff and currently he is a Principal Engineer working on serial link design for mobile and home applications. His research interest include clock generator, high-speed IO, clock and data recovery circuit.

Sang-Hyun Lee received B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1988, 1990, and 2002, respectively.

He joined System-LSI Division, Samsung Electronics, Hwasung, Korea, in 2013 as a Vice President. He is responsible for the development of high speed interface IPs, Link controllers, and Security IPs, bringing the leading edge IPs for mobile processors, memory, display, image, etc. Before joining Samsung, he was with Silicon Image, Xilinx, and nVidia, developing various kinds of interface IPs for TVs, FPGAs, graphic processors, and mobile processors.

Byungsub Kim (M’11) received the B.S. degree in electronic and electrical engineering (EEE) from Pohang University of Science and Technology (POSTECH), Pohang, Korea, in 2000, and the M.S. and Ph.D. degrees in electrical engineering and computer science (EECS) from Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2004 and 2010, respectively. From 2010 to 2011, he worked as an analog design engineer at Intel Corporation, Hillsboro, OR, USA. In 2012, he joined the faculty of the department of Electronic and Electrical Engineering at POSTECH, where he is currently working as an assistant professor. He received several honorable awards. In 2011, Dr. Kim received MIT EECS Jin-Au Kong Outstanding Doctoral Thesis Honorable Mentions, and 2009 IEEE JOURNAL OF SOLID-STATE CIRCUITS Best Paper Award. In 2009, he received Analog Device Inc. Outstanding Student Designer Award from MIT, and was also a corecipient of the Beatrice Winner Award for Editorial Excellence at the 2009 IEEE Internal Solid-State Circuits Conference.

Hong-June Park (M’88–SM’13) received the B.S. degree from the Department of Electronic Engineering, Seoul National University, Seoul, Korea, in 1979, the M.S. degree from the Korea Advanced Institute of Science and Technology, Taejon, in 1981, and the Ph.D. degree from the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA, USA, in 1989. He was a CAD engineer at ETRI, Korea, from 1981 to 1984 and a Senior Engineer in the TCAD Department of INTEL from 1989 to 1991. In 1991, he joined the Faculty of Electronic and Electrical Engineering, Pohang University of Science and Technology (POSTECH), Gyeongbuk, Korea, where he is currently Professor. His research interests include CMOS analog circuit design such as high-speed interface circuits, ROIC of touch sensors and analog/digital beamformer circuits for ultrasound medical imaging. Prof. Park is a Member of IEEK. He served as the Editor-in-Chief of the Journal of Semiconductor Technology and Science, an SCIE journal (http://www.jsts.org) from 2009 to 2012, also as the Vice President of IEEK in 2012 and as the Technical Program Committee Member of ISSCC, SOVC, and A-SSCC for several years. He is the recipient of the 2012 Haedong Academic Award from IEEK and Haedong foundation.

Jae-Yoon Sim (M’02–SM’13) received the B.S., M.S., and Ph.D. degrees in electronic and electrical engineering from Pohang University of Science and Technology (POSTECH), Korea, in 1993, 1995, and 1999, respectively. From 1999 to 2005, he worked as a Senior Engineer at Samsung Electronics, Korea. From 2003 to 2005, he was a Postdoctoral Researcher with the University of Southern California, Los Angeles, CA, USA. From 2011 to 2012, he was a Visiting Scholar with the University of Michigan, Ann Arbor, MI, USA. In 2005, he joined POSTECH, where he is currently an Associate Professor. He has served in the Technical Program Committees of the International Solid-State Circuits Conference (ISSCC), Symposium on VLSI Circuits, and Asian Solid-State Circuits Conference. He is a corecipient of the Takuo Sugano Award at ISSCC 2001. His research interests include high-speed serial/parallel links, PLLs, data converters, and power module for plasma generation.
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