Voltage and Power Balance Control for a Cascaded Multilevel Solid State Transformer

Tiefu Zhao, Gangyao Wang, Jie Zeng, Sumit Dutta, Subhashish Bhattacharya and Alex Q. Huang
Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Center
North Carolina State University
Raleigh, NC 27695, USA
Email: {tzhao, gwang3, jzeng2, sdutta2, sbhatta4, aqhuang}@ncsu.edu

Abstract—In this paper, a 20kVA Solid State Transformer (SST) based on 6.5kV IGBT is proposed for interface with 7.2kV distribution system voltage. The proposed SST consists of a cascaded multilevel AC/DC rectifier stage, a Dual Active Bridge (DAB) converter stage with high frequency transformers and a DC/AC inverter stage. Based on the single phase d-q vector control, a novel control strategy is proposed to balance the rectifier capacitor voltages and the real power through the DAB parallel modules. Furthermore, the power constraints of the voltage balance control are analyzed. The SST switching model simulation demonstrates the effectiveness of the proposed voltage and power balance controller. A 3kW SST scale-down prototype is implemented. The experiment results verify the single phase d-q vector controller for the SST cascaded multilevel rectifier.

I. INTRODUCTION

The Solid State Transformer (SST) is one of the key elements in the proposed Future Renewable Electric Energy Delivery and Management (FREEDM) Systems. In the electric configuration of the FREEDM system shown in Fig.1, low voltage (120V), residential class Distributed Renewable Energy Resource (DRER), Distributed Energy Storage Device (DESD), and loads are connected to the distribution bus (12kV) through a power electronics based Intelligent Energy Management (IEM) subsystem.

The solid state transformer is within the IEM and used to enable active management of DRER, DESD and loads, rather than a 60Hz conventional transformer. The SST has the features of instantaneous voltage regulation, voltage sag compensation, fault isolation, power factor correction, harmonic isolation and DC output [1-3]. The SST will have a 400V DC port that will facilitate more efficient connection of certain classes of DRERs and DESDs. Acting very much like an energy router, each SST will have bi-directional energy flow control capability allowing it to control active and reactive power flow and to manage the fault currents on both the low voltage and high voltage sides. Its large control bandwidth provides the plug-and-play feature for distributed resources to rapidly identify and respond to changes in the system.

In order to direct interface with the 12kV distribution voltage level, series devices or multilevel converter modules are still required due to today’s semiconductor voltage level (6.5kV for silicon device and 10kV for SiC MOSFET). This paper proposes a 20kVA SST based on the cascaded H-Bridge multilevel rectifier to reach the required voltage levels. One of the main disadvantages of the cascaded H-Bridge rectifier is the voltage unbalance on the DC bus voltages of different H-Bridges. The similar voltage unbalance issue was addressed in the cascaded H-Bridge inverter based STATCOM and drive applications [4-7]. In the STATCOM application, where the rectifier is used for reactive power compensation, the references use low frequency optimal PWM modulation technique, so the voltage balance is realized by shifting the voltage waveforms. In contrast, drive application generally transfers real power. In the references, the DC bus voltage is balanced by using different switching patterns to charge and discharge each H-Bridge capacitor, but the reactive power is not controlled. Differently from the STATCOM and drive application, the SST requires a high frequency modulation and both real and reactive power control. Therefore, the voltage

This work was supported by ERC Program of the National Science Foundation under Award Number EEC-08212121.
balance and power balance control is indispensible for the SST controller design.

In this paper, the modeling of the SST, including AC/DC rectifier, dual active bridge converter are developed. A single phased d-q vector controller is applied in the rectifier stage to control both the real and reactive power. Based on the single phase d-q control, a voltage balance control method is proposed to solve the voltage unbalance that could appear on the DC voltages of different H-bridges. Meanwhile, a power balance control method is proposed to regulate the real power transferring through the DAB parallel modules. The proposed voltage and power control is verified by the switching model simulation. A 3kW SST scale-down prototype is implemented by using 600V IGBT. The SST prototype experiment also verifies the single phase d-q vector control.

A. Rectifier single phase d-q vector control

The AC/DC rectifier stage converts the single phase 7.8kV AC voltage to three DC output while controlling the reactive power at the input side. The rectifier consists of three cascaded H-bridges with each reference DC bus voltage 3.8kV. The average differential equations of the rectifier are:

\[
\frac{di_a}{dt} = \frac{3E}{L_s} d_a - \frac{V_{pccm}}{L_s} \frac{R_s}{L_s} i_a
\]

\[
\frac{dE}{dt} = -\frac{E}{R_s C} \frac{d_i}{C} a
\]

Where, \(i_a\) is the input side current, \(V_{pccm}\) is the input voltage, \(R_s\) is the input line resistance, \(L_s\) is the input inductor, \(E\) is the DC bus voltage, \(C\) is the rectifier DC capacitor, \(d_a\) is the rectifier PWM duty cycle.

The single phase d-q vector control is applied in the rectifier controller. An imaginary phase M which is 90 degree lagging the original phase A is hypothesized. The differential equations for the imaginary phase are:

\[
\frac{di_m}{dt} = \frac{3E}{L_m} d_m - \frac{V_{pccm}}{L_m} \frac{R_s}{L_m} i_m
\]

\[
\frac{dE_m}{dt} = -\frac{E_m}{R_m C} \frac{d_{im}}{C}
\]

Where, \(i_m\) is the input current of the imaginary phase, \(V_{pccm}\) is the input voltage of the imaginary phase, \(E_m\) is the DC bus voltage of the imaginary phase, \(d_m\) is the rectifier PWM duty cycle of the imaginary phase. Based on the small ripple approximation, \(E_m = E \cdot i\). Then combine the equations for two phases, and rewrite the equations:

\[
\frac{di_{am}}{dt} = \frac{3E}{L_s} d_{am} - \frac{V_{pccam}}{L_s} \frac{R_s}{L_s} i_{am}
\]

\[
\frac{dE_{am}}{dt} = -\frac{E_{am}}{R_s C} \frac{d_{im}}{2C}
\]

Where,

\[
i_{am} = \begin{bmatrix} i_a \\ i_m \end{bmatrix}, \quad d_{am} = \begin{bmatrix} d_a \\ d_m \end{bmatrix}, \quad V_{pccam} = \begin{bmatrix} V_{pcca} \\ V_{pccm} \end{bmatrix}
\]

The single phase d-q transformation is applied to the equations (5) and (6) [8], and the differential equations in d-q coordinates are derived.

\[
[x]_{dq} = [T]\cdot [x]_{am}
\]
Where,
\[ T = \begin{bmatrix} \sin(\theta) & -\cos(\theta) \\ \cos(\theta) & \sin(\theta) \end{bmatrix}, \theta = 2\pi f_L , f_L \text{ is line frequency.} \]

Then the d-q axis equation of the single phase H-bridge rectifier is given in equation (8) and (9).

\[
\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{3E}{L_s} \begin{bmatrix} d_d \\ d_q \end{bmatrix} - \frac{1}{L_s} \begin{bmatrix} v_{pced} \\ v_{pcq} \end{bmatrix} - \frac{R_s}{L_s} \begin{bmatrix} -\omega \\ \omega \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix}
\]

(8)

\[
\frac{dE}{dt} = -\frac{E}{R_LC} - \frac{1}{2C} \begin{bmatrix} d_d \\ d_q \end{bmatrix}^T \begin{bmatrix} i_d \\ i_q \end{bmatrix}
\]

(9)

With the chosen PLL, the voltage vector is aligned with the direction of the d-axis during steady state. The grid voltage component in the d-direction is equal to its peak value and the q-component of the grid voltage is equal to zero. Thus, the d-component of the current vector (in steady state parallel to the grid voltage vector) becomes the active current component (d-current) and the q-component of the current vector becomes the reactive current component (q-current) [9]. The decoupled d-q vector controller for each H-bridge is shown in Fig. 3. The three SPWM carriers for the cascaded H-bridge are phase shifted so that the rectifier has seven voltage levels to reduce the voltage stress and harmonics.

The control aim of the controller is to control the reactive power (or power factor) and regulate the DC bus voltage. The two PI regulators in d-q axis loop are designed based on the bode plots.

**B. Modeling and Control of DAB**

The Dual Active Bridge (DAB) consists of a high voltage H-Bridge, a high frequency transformer and a low voltage H-bridge. The rectifier regulates the high voltage DC link voltage and controls the input current to be sinusoidal from the AC input. The low voltage DC link is regulated by the DAB converter.

The dual active bridge topology offers zero voltage switching for all the switches, relatively low voltage stress for the switches, low passive component ratings and complete symmetry of configuration that allows seamless control for bidirectional power flow. Real power flows from the bridge with leading phase angle to the bridge with lagging phase angle, the amount of power transferred being controlled by the phase angle difference and the magnitudes of the DC voltages at the two ends as given by equation (10). [10]

\[ P_o = \frac{V_{dc} V_{dc\_link}}{2f_H} d_{dc} (1 - d_{dc}) \]

(10)

where, \( V_{dc} \) is input side high voltage DC voltage, \( f_H \) is switching frequency, \( L \) is leakage inductance, \( V_{dc\_link} \) is output side low voltage DC link voltage referred to input side and \( d_{dc} \) is ratio of time delay between the two bridges to one-half of switching period.

For the DAB converter, the phase shift control is used to regulate the low voltage DC voltage to the reference 400V under different load conditions. First the difference between the low voltage DC voltage \( V_{dc} \) and the reference voltage is compared. Then the phase shift angle is adjusted by the PI controller to regulate \( V_{dc} \) according to this voltage error.

![Fig. 4 (a) Dual active bridge circuit (b) DAB voltage controller](image)

**III. VOLTAGE AND POWER BALANCE CONTROL**

Since the rectifier stage of the SST consists of three H-Bridges in series, the voltage unbalance could appear on the DC bus voltages (E1, E2, and E3, shown in Fig. 5) due to the device loss mismatching and H-Bridge real power difference. The unbalanced voltage may result in capacitor over-voltage.

The DAB stage consists of three DAB modules in parallel. The power unbalance (P1, P2 and P3, shown in Fig.5) can be caused by the transformer parameter (leakage inductance or turns ratio) mismatching and DC bus voltage differences. The power unbalance may cause device over-current issue.
A. Voltage balance control

The single phase d-q vector controller for the rectifier stage regulates the total DC bus voltage and controls the reactive power. Based on the single phase d-q control, a voltage balance control method is proposed to solve the voltage unbalance on the DC voltages of different H-bridges.

In Fig. 6, the $d_d$ and $q_d$ are calculated according to the single phase d-q vector control. Fig. 7 is the voltage balance controller, the individual DC bus voltages of the first two H-bridges, $E_1$ and $E_2$, are compared with the DC bus voltage reference $E_{ref}$ to generate a d-axis compensation $\Delta d_{d1}$ and $\Delta d_{d2}$ by a PI regulator. Then $\Delta d_{d1}$ and $\Delta d_{d2}$ are added to the original $d_d$. Therefore, $d_{d1}$ for the first H-Bridge and $d_{d2}$ for the second H-Bridge are adjusted so that the real power of each H-Bridge can be changed. The real power of the H-Bridge with a lower (or higher) DC bus voltage is increased (or decreased) to eliminate the voltage unbalance.

For the third H-Bridge, $\Delta d_{d3} = -\Delta d_{d1} - \Delta d_{d2}$, so the total DC bus voltage is still regulated.

The switching model simulation of the 20kVA SST cascaded H-Bridge rectifier is implemented in Matlab/Simulink. In the simulation, different resistor loads are connected to the DC buses, $E_1$, $E_2$, and $E_3$. The resistor loads $R_1 = 1.0$ pu, $R_2 = 0.8$ pu, $R_3 = 1.0$ pu (20% load unbalance). Fig. 8 shows the three DC bus voltages without balance control. The H-Bridge which transfers more power has the highest DC bus voltage. Fig. 9 shows the three DC bus voltages with balance control. The three DC bus voltages are equal in the steady state.
B. Voltage balance constraints

In the proposed voltage balance controller, the real power of each H-Bridge is adjusted to eliminate the DC bus voltage unbalance. However, the adjustable real power range of each H-Bridge is limited by the input AC voltage and the DC bus voltage reference. In the designed SST system, the input voltage is 7.2kV and each DC bus voltage reference is 3.8kV. As shown in Fig. 10, the constraints of the voltage vectors are given by equation (10)-(15).

\[ V_1 + V_2 + V_3 = V_{\text{line}} + jωL \]  
\[ V_{d1} + V_{d2} + V_{d3} = V_{\text{line}} = 3 \times 3.8kV \]  
\[ V_{d1} \leq |V| = d_1E_1 = d_1 \times 3.8kV \leq 3.8kV \]  
\[ V_{d3} \leq |V| = d_3E_3 = d_3 \times 3.8kV \leq 3.8kV \]  
\[ V_{d2} \leq |V| = d_2E_2 = d_2 \times 3.8kV \leq 3.8kV \]  

From the above equations, the voltage vector constraints for the voltage d-axis components Vd1, Vd2 and Vd3 are given by equation (16)-(18).

\[ 2.6kV \leq V_{d1} \leq 3.8kV \]  
\[ 2.6kV \leq V_{d2} \leq 3.8kV \]  
\[ 2.6kV \leq V_{d3} \leq 3.8kV \]  

The real power of each H-Bridge is calculated as:

\[ P_1 = I_{\text{line}}V_{d1}, P_2 = I_{\text{line}}V_{d2}, P_3 = I_{\text{line}}V_{d3} \]  

Therefore, the real power range of each H-Bridge is:

\[ 2.6kV \times I_{\text{line}} \leq P_1 \leq 3.8kV \times I_{\text{line}} \]  
\[ 2.6kV \times I_{\text{line}} \leq P_2 \leq 3.8kV \times I_{\text{line}} \]  
\[ 2.6kV \times I_{\text{line}} \leq P_3 \leq 3.8kV \times I_{\text{line}} \]  

In order to balance the DC bus voltages, the real power of each H-Bridge has to be within the range in equation (20) - (21). Based on the above analysis, when Vd1=Vd2=3.2kV, Vd3=3.8kV, a maximum 15% power unbalance is allowed to maintain the balanced DC buses. Therefore, the power balance control is needed to guarantee the H-Bridge power meets the constraints.

C. Power balance control

Due to the parameter variation of the high frequency transformers, such as leakage inductance and turns ratio, the three DAB currents can be different, which results in a power unbalance of the three DAB modules. A power balance control method is proposed to regulate the real power transferring through the DAB parallel modules. As shown in Fig. 11, the voltage regulator compares the low voltage DC voltage \( V_{dcL} \) with the reference \( V_{dcL\_ref} \) and generates the power references \( P_{\text{ref}} \) for the three DAB modules. Then the power regulator compares the calculated average power of each DAB module with \( P_{\text{ref}} \) and generates the phase shift angles \( ϕ_1, ϕ_2, ϕ_3 \) for the three DAB modules. Fig. 12 shows how the average power calculator calculates the average power in each switching cycle (3 kHz). In the calculation, \( P = \frac{1}{3} \int V_{dcH}I_{dcH}\,dt \), the primary DC voltage \( V_{dcH} \) can be considered constant in a switching cycle. So the power calculation only involves the summation of current, which is easy to be implemented in DSP.

\[ V_{dcH} \]  
\[ K_ϕ + \frac{K_ϕ}{\pi} \]

Fig. 10 Rectifier voltage vector constrains

Fig. 11 Power balance controller
The switching model simulation is implemented to verify the proposed power balance control. In the simulation, different leakage inductance values are set for the three transformers: 165mH, 165mH, 115mH (30% variation). Fig. 13 and Fig. 15 are the DAB primary currents and power without power balance control. The DAB module with smaller leakage inductance has large current and transfers more power. Fig. 14 and Fig. 16 illustrate the DAB primary currents and power with power balance control. The power transferring through each DAB module is balanced.

IV. SST HARDWARE PROTOTYPE

To develop the SST controller and verify the proposed strategy, a scale-down SST prototype is implemented. Fig. 17 and Fig. 18 are the SST single module topology and prototype photo respectively.

The SST module prototype is designed as single phase input voltage 60Hz, 240V, and DC output 400V. Each module consists of an AC/DC rectifier that converts 60Hz, 240V AC to 400V DC bus, a DC/DC converter that convert 400V to 400V DC bus with 1:1 high frequency transformer. The SST module output will connect to a DC/AC inverter that converts 400V DC to 120/240V AC. The prototype is implemented by using 600V 75A Intelligent Power Modules (IPM). The SST control algorithm is programmed in DSP TMS320F28335. The experiment parameters are shown in Table. I. The single phase d-q vector control is implemented in the DSP controller by using model based program. The phase A voltage is delayed by 1/4 cycle to synthesize the imaginary phase M. In the experiment, the DC bus voltage reference is 50V and the reactive power reference is zero, which means a unity power factor. Fig. 19 demonstrates the experiment results of the SST rectifier stage with single phase d-q vector controller. The DC bus voltage is regulated to the reference and the input current is in phase with the input voltage. The
experiment results verify the single phase d-q vector control for the SST.

The 3kW SST scale-down prototype experiment is implemented and verifies the single phase d-q vector controller.

V. CONCLUSIONS

In this paper, a 20kVA Solid State Transformer (SST) based on 6.5kV IGBT is proposed to interface with 7.2kV distribution system and enable active power management of DRER, DESD and loads in the Future Renewable Electric Energy Delivery and Management (FREEDM) System. The single phase d-q vector control is applied to the cascaded H-Bridge rectifier in SST. A novel voltage control strategy is proposed to balance the rectifier capacitor voltages. The constraints of the voltage balance control for the cascaded H-Bridge rectifier is analyzed in details. A power balance control is proposed to balance the real power through the DAB parallel modules. The SST switching model simulation verifies the proposed voltage and power balance controller.

TABLE I. SST PROTOTYPE PARAMETERS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input inductance</td>
<td>1mH</td>
</tr>
<tr>
<td>Primary DC Capacitor</td>
<td>900μF</td>
</tr>
<tr>
<td>Primary DC voltage reference</td>
<td>400V</td>
</tr>
<tr>
<td>Secondary DC Capacitor</td>
<td>900μF</td>
</tr>
<tr>
<td>Secondary DC voltage reference</td>
<td>400V</td>
</tr>
<tr>
<td>Transformer turns ratio</td>
<td>1:1</td>
</tr>
<tr>
<td>Transformer magnetizing inductance</td>
<td>27mH</td>
</tr>
<tr>
<td>Transformer leakage inductance</td>
<td>3mH</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>10kHz</td>
</tr>
</tbody>
</table>

REFERENCES


