Abstract—This paper studies two different methods for the partial DC link voltage balancing of the three-level unidirectional rectifier having supply neutral connection at DC link midpoint. In the first balancing method an additional balancing inductor leg is used to control the partial DC link voltages. The other method balances the voltages by drawing asymmetrical, quasi-sinusoidal phase currents from the utility. The analysis and the functioning of the balancing methods are verified with measurements from 10 kW 230V / 400V 50 Hz laboratory prototype. The control system and the modulator are realized with Freescale MPC563 single-chip microcontroller.

I. INTRODUCTION

The tree-phase/level/switch Vienna I rectifier has been found very suitable topology for three-phase active rectification when only unidirectional power flow is needed. [1]–[3]. It has better efficiency, fewer active switches and smaller AC-filter size compared to conventional six-switch full bridge PWM rectifier. If the rectifier is applied to transformerless double-conversion AC-DC-AC UPS system the supply neutral needs to be connected to the system in order to feed single-phase loads. Moreover, the supply neutral is connected to the DC link midpoint in order to prevent it from floating and thus generating a fault current path via earth connection from the load side [4]. The main circuit of four-wire connected Vienna rectifier (VIENNA4) is presented in Fig. 1. The purpose of the rectifier is to draw sinusoidal currents from the utility with unity power factor.

Figure 1. Main circuit of the four-wire Vienna rectifier with additional DC link balancing circuit.
current consumption mode [5] and an additional balancing circuitry can be applied to the space vector modulated and vector controlled VIENNA4.

II. SPACE VECTOR MODULATION

The space vector modulation method for VIENNA4 has been presented in detail in [8]. A voltage space vector for arbitrary three-phase voltages is defined

\[ u_{ref} = u_a + ju_b = \frac{2}{3}(u_a + a u_b + a^2 u_c), \text{ where } a = e^{j2\pi/3}. \]  \hspace{1cm} (1)

The definition of the space vector does not contain the definition of zero sequence component (ZSC). Therefore the ZSC of space vector is defined separately. The ZSC of arbitrary three-phase voltages is defined

\[ u_z = \frac{1}{3}(u_a + u_b + u_c). \]  \hspace{1cm} (2)

Possible space vectors of VIENNA4 are presented in Fig. 2. There are a total of 19 different voltage vectors available in the complex plane. Each of the six small vectors \( u_{01} - u_{06} \) can be produced with two alternative switching combinations that realize the same voltage vector in complex plane but the ZSCs of the alternative combinations are of opposite sign and magnitude. These alternative and redundant small vectors are denoted \( u_{0n}(+, -) \), where \( u_{0n}^+ \) and \( u_{0n}^- \) refer to the sign of the ZSC of the redundant vector.

A. Space Vector Modulation in Complex Plane

The principle of the reference voltage vector realization in main sector I is presented in Fig. 3. Each main sector I-VI presented in Fig. 2 is divided into four subsectors 1 – 4 (Fig. 3). The subsectors are the areas defined by the nearest three vectors (NTV). An arbitrary voltage reference vector \( u_{ref} \) can be realized by proper weighting of the NTV i.e.

\[ u_{ref} = d_1 u_1 + d_2 u_2 + d_3 u_3, \]  \hspace{1cm} (3)

where \( u_{1(2,3)} \) are the NTV of the reference and the \( d_{1(2,3)} \) are the duty cycles of the NTV. The duty cycles can be determined by assuming equal DC link capacitor voltages and calculating the glancing projections \( u_\kappa \) and \( u_\lambda \) of the reference vector to the main vectors that outline the main sector in question. The projections are

\[ u_\kappa = |u_{ref}| \left( \cos(\varphi_{ref,sec}) - j \sin(\varphi_{ref,sec}) / \sqrt{3} \right), \]  \hspace{1cm} (4)

\[ u_\lambda = |u_{ref}| 2 \sin(\varphi_{ref,sec}) / \sqrt{3}, \]  \hspace{1cm} (5)

where \( \varphi_{ref,sec} \) is the angle of the reference vector \( u_{ref} \) inside the main sector in question. The projections are scaled with the length of the small vectors \( (U_{dc}/3) \) to get the normalized duty cycles \( d_\kappa \) and \( d_\lambda \) which are used to identify the subsector of the reference voltage \( u_{ref} \) [9] and to determine the duty cycles of the NTV.

\[ d_\kappa = \frac{3 u_\kappa}{U_{dc}}, \]  \hspace{1cm} (6)

\[ d_\lambda = \frac{3 u_\lambda}{U_{dc}}. \]  \hspace{1cm} (7)

The NTV and their duty cycles in main sector I are presented in Table I. For other main sectors the vectors in Table I need to be replaced with similar vectors of the main sector in question.
B. Zero-Sequence Voltage Reference Realization

In each subsector the sequence consists of four voltage vectors: It begins and ends with redundant vectors $u_{0n}$ and $u_{0n+}$, contains one vector that has null ZSC, and one vector that has nonzero ZSC [8]. The zero-sequence voltage reference $u_{z,ref}$ can be realized with proper weighting of the two redundant vector combinations $u_{0n(+,-)}$. The duty cycles of the redundant vectors are weighted with ratio $r$, i.e.

$$d_r = (1 + r) \frac{d_e}{2}$$

$$d_e = (1 - r) \frac{d_e}{2},$$

where $d_e$ is the duty cycle of the redundant vector $u_{0n}$ in the sequence and $-1 < r < 1$. The value of $r$ as a function of zero-sequence voltage reference $u_{z,ref}$ varies in regions A and B (these areas are subscripts of the main sector indices in Fig 2.) and the values are

$$r_A = \frac{2 \left( \frac{d}{d_e} \right)}{3} + \frac{1}{3} + \frac{4u_{z,ref}}{U_{dc} \cdot d_e}$$

$$r_B = \frac{4u_{z,ref}}{U_{dc} \cdot d_e} - \frac{2 \left( \frac{d}{d_e} \right)}{3} - \frac{1}{3},$$

where $d_e$ is the duty cycle of the vector having nonzero ZSC in the sequence.

III. BALANCING METHODS

A. Load Asymmetry

The supply neutral connection at the midpoint (Fig.1) changes the rectifier phase operation compared to three-wire connected rectifier. Each phase is modulated with respect to neutral and the states of the other phases do not affect to the resulting individual phase voltage $u_{kN}$, where $k = a, b, c$. During the positive half-cycle the rectifier phase voltage $u_{kN}$ can have two values: $U_{Cdc1}$ and 0. During the negative half-cycle $u_{kN}$ can have values $-U_{Cdc2}$ and 0 respectively.

The relative asymmetry of the DC link load in Fig. 1 is defined [10]

$$\alpha_{rel} = \frac{P_2 - P_1}{P_{dc}},$$

where $P_{dc}$ is the average total power drawn from the DC link, $P_1$ and $P_2$ are the positive and negative average partial DC link load powers, and where $-1 < \alpha_{rel} < 1$.

The value for the load asymmetry can also be obtained by calculating the relative asymmetry from partial the DC link voltages, whose values are inversely proportional to load powers i.e.

$$\alpha_{rel,dc} = \frac{U_{Cdc1} - U_{Cdc2}}{U_{dc}}$$

and approximating the asymmetry with PI controller. This is illustrated in Fig. 4, where the approximated value $\alpha_{rel,c}$ range is the same as in (12) i.e. $-1 < \alpha_{rel,c} < 1$.

B. Balancing Leg

The rectifier DC link with balancing leg is shown in Fig. 5. The balancing leg consists of two IGBT modules (T1 and T2) and an inductor $L_M$. The inductor current $i_{LM}$ can be controlled by controlling the inductor voltage with $T_{1,2}$. When $i_{LM} > 0$ the inductor charges the lower DC link capacitor $C_{dc2}$ with respect to $C_{dc1}$ and when $i_{LM} < 0$ the capacitor $C_{dc1}$ is charged with respect to $C_{dc2}$.

For the power balance between the DC link and the mains side we get (by ignoring the converter losses and assuming unity power factor operation with ideal mains)

$$P_{dc} = P_1 + P_2 = \frac{3}{2} U_\alpha I_\alpha,$$

where $U_\alpha$, $I_\alpha$ are the average direct components (d) of the supply voltage and current in the mains oriented synchronous reference frame. If balanced DC link voltages are desired, the difference of the partial loads $P_{1,2}$ must be compensated with inductor current $I_{LM}$ i.e.

$$I_{LM} \frac{U_{dc}}{2} = P_2 - P_1,$$

By applying (12) and (14) to (15) and approximating the asymmetry with controlled value $\alpha_{rel,c}$ we obtain the value for average inductor current $I_{LM}$ that is needed to compensate the DC link asymmetry

$$I_{LM} = \frac{3U_\alpha I_\alpha}{U_{dc}} \alpha_{rel,c}.$$

The control system for balancing inductor current control is illustrated in Fig. 6. The inductor current reference $i_{LM,ref}$ is obtained with (16). The measured inductor current $i_{LM}$ is sub-
trated from the reference current $i_{LM,ref}$ and the error is brought to the PI controller that approximates the reference voltage $u_{LM,ref}$ over the inductor $L_M$. The reference voltage is brought to the modulator, which calculates the toggle times $t_{swT(1,2)}$ of the switches $T_{1,2}$. The modulator sampling period is $T_s$, during which the switch toggle time instant is calculated. During odd sample periods the switch $T_1$ is toggled ON and $T_2$ is turned OFF. During even periods the $T_1$ is toggled OFF and $T_2$ is turned ON. The toggle times of the switches are

$$t_{swT(1,2)}(i) = \begin{cases} 
1 - \frac{u_{LM,ref} + U_{Cdc2}}{U_{dc}}, & \text{when } T_i \text{ is odd} \\
\frac{u_{LM,ref} + U_{Cdc2}}{U_{dc}} T_i, & \text{when } T_s \text{ is even.}
\end{cases}$$

(17)

This results in the switching frequency $f_{sw} = 1/2T_s$.

C. Quasi-Sinusoidal Current Consumption Mode

The upper DC link capacitor $C_{dc1}$ is charged during positive phase current $i_{d}$ half-cycles and lower capacitor $C_{dc2}$ during negative half-cycles. Therefore the partial DC link capacitor voltages can be controlled by varying the ratio of the rectifier current amplitudes between opposite half-cycles [5]. The half-cycle asymmetry is illustrated in Fig. 7 where the dashed line shows the symmetrical sinusoidal current reference $i_{d,ref}$ and the solid line shows the quasi-sinusoidal reference $i_{d,ref}^{\prime}$ where a bias is added to the positive half-cycle amplitude reference and subtracted from the negative half-cycle amplitude reference.

The difference of the amplitudes needed for the DC link voltage balancing in certain load asymmetry, is obtained by multiplying the positive and negative half-cycle amplitude references with $(1 - \alpha_{rel,c})$ and $(1 + \alpha_{rel,c})$ respectively. Similar asymmetry can be produced if the current controller reference $i_{d,ref}$ is kept sinusoidal and the measured current $i_{d}$ i.e. the feedback for the current controller is manipulated. The relative asymmetry factor $\alpha_{rel,c}$ can be used directly to produce the desired asymmetry by multiplying the measured current value $i_{d}$ with

$$i_{d}^{\prime} = (1 + \alpha_{rel,c})i_{d}, \text{ when } i_{d} > 0$$

$$i_{d}^{\prime} = (1 - \alpha_{rel,c})i_{d}, \text{ when } i_{d} < 0,$$

where $i_{d}^{\prime}$ is the manipulated current feedback. When the manipulated current feedback is fed to the current controller the steady state waveform is similar to that in Fig. 7. The controller controls the manipulated value $i_{d}^{\prime}$ to follow the dashed line and therefore the real current value follows the solid line in Fig. 7.

IV. CONTROL SYSTEM

The space vector modulation method and DC link balancing methods are applied to a vector controlled four-wire Vienna rectifier. The control is performed in mains oriented synchronous reference frame rotating at $\alpha$ s. The space vector voltage equation of the rectifier with L-type filter in the synchronous reference frame is

$$u^{\prime} = L \frac{di^{\prime}}{dt} + j\omega L i^{\prime} + u^{\prime}.$$ 

(19)

Eq. 19 can be expressed in terms of direct (d), quadrature (q) and zero-sequence (z) components, i.e.

$$u_{d} = u_{d} + L \frac{di_{d}}{dt} - \omega L i_{q}$$

(20)

$$u_{q} = u_{q} + L \frac{di_{q}}{dt} + \omega L i_{d}$$

(21)

$$u_{z} = u_{z} + \frac{1}{3} L \frac{di_{z}}{dt}.$$ 

(22)

The control system is derived on the basis of (20), (21) and (22). The simplified block diagram of the control system is presented in Fig. 8.

The phase locked loop PLL is used to track the angle $\varphi_a$ of the synchronous reference frame. Measured line voltages $u_{a,b,c}$ and rectifier currents $i_{d,q,z}$ are transformed into the synchronous reference frame quantities $u_{a,q,z}$ and $i_{d,q,z}$. If the quasi-sinusoidal current control method is used the measured currents $i_{a,b,c}$ are multiplied according to (18) before the transformation. When the balancing leg is in use the measured values are not manipulated. The total DC link voltage difference is brought to a PI controller, which gives the rectifier d-component reference $i_{d,ref}$. The q- and z-component references $i_{q,ref}$, $i_{z,ref}$ are set at zero. The balancing of the partial DC link voltages is carried out by calculating the relative asymmetry of the DC link voltages as in (13) and feeding it through a PI controller that approximates the relative load asymmetry $\alpha_{rel,c}$. The measured rectifier currents $i_{a,b,c}$ are subtracted componentwise from the references $i_{a,b,c,ref}$, and the resulting current error is brought to PI controller, which approximates the filter volt-
age reference $U_{\text{ref},(d,q,z)}$. The filter voltage reference is subtracted from line voltages $U_{(d,q,z)}$ and is brought to block “CCC”, which does the cross-coupling compensation for the d- and q-component voltage equations (20) and (21). The output of the CCC block gives the rectifier voltage reference $U_{r,(d,q,z)}$ in synchronous reference frame, which is then transformed to stationary frame $U_{r,(\alpha,\beta,z)}$ and brought to the modulator. The modulator calculates the duty cycles and the redundant vector weighting factor $r$ and controls the rectifier active switches as described in section II.

If the balancing inductor leg is used the inductor current reference $i_{LM,\text{ref}}$ is calculated in block “bal. cont.” according to (16). The current control is performed in the same block and as an output the block gives the voltage reference $U_{LM,\text{ref}}$ to modulator, which controls the active switches of the balancing leg.

V. EXPERIMENTAL RESULTS

A. Prototype Implementation

The 10 kW rated laboratory prototype of VIENNA4 is presented in Fig. 9. The main circuit consists of three IXYS VUM 25-05E modules, 2200 µH (4.3% p.u.) three phase AC inductor, and two series connected 3.3 mF (16.5 p.u.) aluminium electrolytic capacitors. The balancing leg consists of 5000 µH (9.8% p.u.) AC inductor and Semikron SKM123D IGBT-module. The rectifier is fed from 230 V/400 V 50 Hz utility mains and the DC link voltage reference $U_{\text{dc,ref}}$ is set at 750 V. All main circuit components are connected via copper wires and bus bars. The prototype includes also voltage and current measurement boards that scale the measured quantities to microcontroller A/D converter voltage level 0V – 5V.

The control system and the modulator are both implemented digitally with Freescale MPC563 32-bit single chip microcontroller board. The microcontroller’s time processor unit TPU schedules interrupts every $T_s = 50$ µs time periods in which the modulator is updated. This results in 10 kHz switching frequency for both the rectifier bridge and the balancing leg. In the microcontroller implementation, the control system and the controllers are put into discrete form.

<table>
<thead>
<tr>
<th>load</th>
<th>$P_{\text{load}}$ (kW)</th>
<th>$\alpha_{\text{rel}}$</th>
<th>bal. mode</th>
<th>PF</th>
<th>eff. (%)</th>
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<tr>
<td>symm.</td>
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<td>QSCM</td>
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<td>93.7</td>
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<td></td>
<td></td>
<td></td>
<td>BLM</td>
<td>0.994</td>
<td>94.3</td>
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</table>
B. Measurements

The functioning and validity of the control methods were verified with measurements from the prototype. The load of the rectifier consists of two resistors $R_{(1,2)}$ connected over the DC link as in Fig.1. Five different operating points were chosen to investigate the balancing methods. One was a symmetrical load, where $R_1 \approx R_2$ and four asymmetrical loads, where $R_1 < R_2$. The DC link voltage balancing was tested with both the quasi-sinusoidal current consumption mode (QSCM) and the balancing leg mode (BLM) for the same loads. The load parameters, power factors and efficiencies for all five operating points are presented in Table II for both modes.

The measured waveforms of the rectifier in symmetrical 5.27 kW load are presented in Fig. 10 using QSCM and in Fig. 11 using BLM. The rectifier current waveforms are very similar with both balancing methods due to the absence of the load asymmetry. The total harmonic distortion of phase-a current calculated up to 2 kHz (THD$_{2kHz}$) is 2.5 % in QSCM and 2.4 % in BLM. With both methods the partial DC link voltages are well balanced. The converter efficiency with BLM (93.2 %) is slightly lower than with QSCM (95.7 %) due to the losses in the balancing leg. The balancing leg current in Fig. 11d is nearly zero averaged since there’s no need for voltage balancing. Input power factors are near unity with both examined

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(a) (b) (c)

Figure 10. The measured waveforms of the rectifier operating in 5.27 kW symmetrical load with QSCM. (a) rectifier phase currents $i_{r(a,b,c)}$, THD$_{2kHz} = 2.5 \%$, (b) neutral current $i_n$, (c) partial DC link voltages $U_{Cdc(1,2)}$. 

(a) (b) (c) (d)

Figure 11. The measured waveforms of the rectifier operating in 5.27 kW symmetrical load with BLM. (a) rectifier phase currents $i_{r(a,b,c)}$, THD$_{2kHz} = 2.4 \%$, (b) neutral current $i_n$, (c) partial DC link voltages $U_{Cdc(1,2)}$, (d) balancing leg inductor current $i_{LM}$. 

(a) (b) (c) (d)

Figure 12. The measured waveforms of the rectifier operating in 7.88 kW asymmetrical load with QSCM. (a) rectifier phase currents $i_{r(a,b,c)}$, THD$_{2kHz} = 15.3 \%$, (b) neutral current $i_n$, (c) partial DC link voltages $U_{Cdc(1,2)}$. 

(a) (b) (c) (d)

Figure 13. The measured waveforms of the rectifier operating in 7.88 kW asymmetrical load with BLM. (a) rectifier phase currents $i_{r(a,b,c)}$, THD$_{2kHz} = 1.8 \%$, (b) neutral current $i_n$, (c) partial DC link voltages $U_{Cdc(1,2)}$, (d) balancing leg inductor current $i_{LM}$.
methods (0.989).

The measured waveforms in 7.88 kW asymmetrical load are presented in Fig. 12 with QSCM and Fig. 13 with BLM. Both methods are capable of balancing the capacitor voltages. However, the QSCM causes highly asymmetrical rectifier currents and the power factor drops to 0.941. The phase-a THD_{2kHz} = 15.3 %.

Since the balancing leg is not used the efficiency is reasonably high (96.1 %). By using the BLM the rectifier currents are sinusoidal (Fig. 13) and the power factor is near unity (0.994). The phase-a current THD_{2kHz} = 1.8 %. The efficiency of the converter is 94.3 %, which is lower when compared to QSCM. This is due to the balancing leg and inductor losses.

VI. Conclusion

Two different DC link voltage balancing methods for four-wire Vienna rectifier were studied in the paper. The applied space vector modulation method and control system were presented. Both the quasi-sinusoidal current consumption method and an additional balancing leg were analyzed in detail. The functioning of the balancing methods was verified with measurements from 10 kW laboratory prototype with symmetrical and asymmetrical load conditions. Both examined methods were able to balance the DC link voltages. However, when quasi-sinusoidal mode is used with highly asymmetrical load the utility current quality deteriorates. On the other hand, the additional balancing leg adds more complexity to the circuit and degrades the total efficiency while the utility currents can be kept sinusoidal and balanced regardless of the load asymmetry.

References


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