Ultra-low-noise CMOS current preamplifier from DC to 1 MHz

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An ultra-low-noise, DC–1 MHz, current preamplifier is presented featuring a matched double-MOS architecture around a low offset opamp to obtain bidirectional gain with a signal range from −40 to 30mA. Current noise density reaches a value of 500a/√Hz, equivalent to a 100GΩ resistor, giving a 1pA rms noise in a 1 kHz band. The strictly equal operating point of all transistors ensures excellent linearity even at femto/Ampere input current.

Introduction: A low-noise wideband current preamplifier is the fundamental input stage in those on-chip systems devoted to high resolution measuring applications. Detection of single molecules using nanowires [1], electrical characterisation of nanosamples by means of current-sensing atomic force microscopes [2] or electrical read-out of quantum bits [3] are examples where the nanometric size of the sample produces extremely low current signals and consequently tight requirements to the instrumentation. For these highly critical purposes the preamplifier should feature a very low capacitance at the input node to limit high frequency noise and to allow measurements of fast changing signals (high bandwidth), a continuous-time tracking capability of the input current (DC amplification), the necessary high gain over a wide signal range down to zero current. All these competing requirements are not fully addressed by the available switched amplifiers, lacking of continuous time measurements [4], or by mirror-like architectures, lacking the possibility to work at zero bias [5]. We present a CMOS current preamplifier specifically conceived to address all these points.

Amplifier design: The core of the proposed current amplifier is the matched double-MOS structure shown in the dashed box of Fig. 1(a). Since the four transistors (M1, M2, M2, M3, M4) have the same gate-source voltages and the same gate-drain voltages, the couples M1-M2 and M3-M4 always work in the same operating point. M1 and M2 are composed by N replicas of M1 and M2 transistors, respectively, operating in parallel to give an output current amplified by a factor N irrespective of the transistor nonlinear voltage-current characteristic curves and of any geometrical dependence of the transistor parameters. This double-MOS scheme, derived from the reset networks used in charge preamplifiers [6], ensures bidirectional current amplification by a factor N and extends the capabilities to sub-pA currents by operating the transistors in subthreshold regime.

![Fig. 1 Proposed scheme of current amplifier, and experimental frequency response of two cascaded stages with N1 = 99 and N2 = 10](image)

As the feedback transistors M1M4 are biased only by the input current, in our case ranging from 0 to tens of nA, the loop gain would depend on the input signal. To ensure feedback stability independently of the input current, a capacitor C1 = 100 fF in parallel to M1/M4 has been added, the value of which is chosen sufficiently large to bypass the transistors M1 and M2 at high frequency, giving a loop gain proportional to C1/(C1 + Cm) and an overall bandwidth of the preamplifier equal to GBP C1/(C1 + Cm), where GBP is the gain-bandwidth product of the opamp. A second capacitor C2 is in parallel to M1, and M2 allows keeping a constant current gain over the full bandwidth of the preamplifier. A non-minimal transistor size of M1 and M4 has been chosen to maintain the difference from the low frequency gain (given by the transistors) and the high frequency gain (given by the capacitors) at less than 1.5% in the worst case. The optimal transistors size (reported in Fig. 1a) has been selected by Monte-Carlo simulations taking into account the constraint of a total input capacitance of the preamplifier less than 1pF to ensure a bandwidth of 1 MHz and a low noise. A total current gain of 990 has been obtained by cascading two stages with gain N1 = 99 and N2 = 10, respectively.

Noise and non-ideal effects: While providing gain and a wide signal range, the transistors M1/M4 in the feedback loop also ensure low noise. Indeed, by operating in subthreshold regime over the entire input signal range, they contribute with a small flicker noise (frequency corner of only few Hz) and a shot noise term (2qIN) that scales adaptively with the input current, down to less than 1fA/√Hz when input current is lower than 3 pA. The noise voltage $V_n^2$ of the opamp over the input capacitances (C1+Cm) sets the minimum noise of the system when $I_n$ is very low (<1 pA), as can be seen from the input referred current noise:

$$I_n = I_0 + \frac{W}{L} V_T e^{\frac{V_S}{V_T}} G_{in} + \frac{2}{\pi} f_0 (C_1 + C_m) f^2 V_n^2$$

In multiple stage amplifiers, the noise is set by the first stage provided that the gain of the first one is sufficiently high, as in our case.

A mismatch between transistors 1 and 2 and/or an offset voltage of the opamp that imposes different operating points to transistors 1 with respect to transistors 2 are possible sources of non-idealities. Their effect can be analysed by recalling the drain current in subthreshold regime (for an n-channel transistor):

$$I_D = I_{00} W \frac{1}{L} e^{\frac{V_S}{V_T}} G_{in} + \frac{2}{\pi} f_0 (C_1 + C_m) f^2 V_n^2$$

where $K$ is a constant depending on the size of the transistor and on the threshold voltage, $V_T = kT/q$ is the thermal voltage and $\alpha$ is the subthreshold gate coupling coefficient. The source voltage $V_S$, the only parameter changing with the input current, is exactly the same for $M_1$ and $M_2$, ensuring a highly linear input-output characteristic, as previously mentioned. The offset voltage of the opamp instead, sets the drain voltage $V_D$, giving a constant current that adds to the input signal. In our prototype this value is less than 10fA and can be further reduced by a DC calibration or by a careful low offset opamp design. The statistical dispersion of the technological parameter $K$ is reflected only on the gain value and has been limited by proper sizing of transistors as previously discussed.

Experimental results: Made using standard 0.35 μm CMOS technology, the amplifier occupies 0.48 mm² and works with a dual ±1.5V power supply. The gain (990), bandwidth (1 MHz) and flatness of the transfer function (less than 1% up to 100 kHz) can be extracted from the measured transfer function of Fig. 1(b) obtained with an input capacitance of 5pF. The output current has been measured using an external transimpedance amplifier (see Fig. 1a) with feedback resistance of $R_F = 100 \Omega$ that adds an equivalent input noise of 500 aA/√Hz to (1) and a flicker noise with a corner frequency of 10 Hz. The high linearity of the stage over the full dynamic range and down to fA input currents together with the symmetry between positive and negative signals are confirmed by the result reported in Fig. 2. Fig. 3 reports the measured noise and expected values showing a sub-fA/√Hz for low input currents (<500 fA). The rms noise on 1 MHz bandwidth is 20pA rms, reducing to only 1pA rms for a smaller bandwidth of 100 kHz. The low frequency noise can be further reduced by improving the external transimpedance amplifier and/or by increasing the gain of the preamplifier. For higher current the white noise recovers shot noise behaviour as reported in Fig. 3 (inset) and as predicted by (1). Note that a simple feedback resistor with a value $R = 1.5 \times 10^7 \Omega$ at 50 MHz (chosen to avoid the opamp saturation at the maximum input current) would give a noise of 18 fA/√Hz, more than 20 times the minimum noise measured on our prototype.
Conclusion: A simple CMOS current preamplifier based on replicating N times the input devices is presented. The experimental characterisation certifies how the very good matching capability of the CMOS technology allows the architecture to reach a nearly perfect compensation of the nonlinearity giving a highly linear amplifier also for fA currents. The result is an amplifier operating up to 30nA from DC to 1 MHz, with a noise reaching a minimum value equivalent to the thermal noise of a 100GΩ resistor.

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References