A 16nm FinFET CMOS Technology for Mobile SoC and Computing Applications


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Abstract
For the first time, we present a state-of-the-art energy-efficient 16nm technology integrated with FinFET transistors, 0.07um² high density (HD) SRAM, Cu/low-k interconnect and high density MiM for mobile SoC and computing applications. This technology provides 2X logic density and >35% speed gain or >55% power reduction over our 28nm HK/MG planar technology. To our knowledge, this is the smallest fully functional 128Mb HD FinFET SRAM (with single fin) test-chip demonstrated with low Vccmin for 16nm node. Low leakage (SVt) FinFET transistors achieve excellent short channel control with DIBL of <30 mV/V and superior Idsat of 520/525 uA/um at 0.75V and Ioff of 30 pA/um for NMOS and PMOS, respectively.

Introduction
As CMOS technology continues to advance, FinFET device has been commonly recognized as one of the promising candidates to replace planar device thanks to its excellent electrostatic and short channel control. This paper presents a leading edge FinFET technology for high volume production with optimal process complexity and cost. Competitive SRAM bit cells are designed to provide the optimized standby, cell current and Vccmin. FinFET transistors with multi-Vts are offered to provide design flexibility for wide spectrum applications. High precision resistor, MOS varactors, parasitic BJT and diodes are also offered to enable analog/mixed signal design. Cu/low-k interconnect with different metal combinations of metal thickness and pitch provides balanced R/C and routing density. The planar MiM with high-k dielectric offers high density on-chip capacitor >20F/um² for noise reduction. Key technology features are summarized in Table I.

Process Architecture
Fin patterning and formation on bulk with 48nm fin pitch is realized using pitch-splitting technique where fin width is determined by the sidewall thickness of a mandrel. Poly-silicon deposition and gate patterning with gate pitch of 90nm on 3-D fin structure is followed by HK/MG RPG process. Raised source/drain with dual epitaxy process is used and optimized to mitigate S/D parasitic resistance. MEOL with W plug provides local routing connected to gate and source/drain. M1 / Mx metal pitch of 64nm is enabled using advanced patterning scheme, whereas single patterning is adopted for metal pitch of 80nm/90nm and above. Cu/low-k process is optimized to have balanced R/C and sufficient manufacturing margin.

Transistor Performance
FinFET transistors with HK/MG are optimized for low power and high performance applications. Figure of Merits (FOM) based on a combination of Inverter, NAND, and NOR with F.O.=-3 illustrate >35% speed gain at the same total power or >55% power reduction at the same speed over our 28nm HK/MG planar transistors in Fig. 2. Excellent transistor Ion-Ioff characteristics of uLVt/LVt devices with Lg=30nm, and SVt devices with Lg=34nm are shown in Fig. 3 & 4. Both NMOS and PMOS transistors outperform previously reported FinFET and FDSOI transistor data [1-3]. Additional devices with gate pitch of 106nm (Lg=50nm) are available for further off-state leakage reduction down to 10pA/um. Fig. 5 shows the Id-Vg characteristics of multi-Vt transistors. SVt transistors (Lg=34nm) achieve sub-threshold swing of <65 mV/dec. and DIBL of <30 mV/V with Idsat of 520/525 uA/um at 0.75V and Ioff of 30pA/um for NMOS and PMOS, respectively.

Analog Characteristics
FinFET process offers excellent analog characteristics. The 28nm HKMG planar process as the reference. Comparing to the reference process, FinFET transistors demonstrate similar or better 1/f noise characteristics for NMOS and PMOS, as shown respectively in Fig.6a & 6b. Reduction of MOSFET Vt mismatch (AVt) by 36% and 24% for FinFET NMOS and PMOS, respectively, is achieved as illustrated in Fig.7a & 7b. In addition, as compared to the reference devices, FinFET NMOS and PMOS is seen to achieve 1.9X / 1.4X enhancement of current efficiency (gm/Id) and 3.1X / 2.7X improvement of intrinsic voltage gain (gm/gds), as shown in Fig.8. For passive devices, High-R precision resistor with...
mismatch <0.3%-um is offered. FinFET process is also capable of enabling core and I/O MOS varactors with high capacitance density and capacitance tuning ratio of 7.5 & 4.4, respectively, as shown in Fig.9.

**SRAM and Interconnect**

Competitive HD, HC and HP SRAM cells are designed and optimized for low leakage, high performance and low Vccmin applications. HD/HC SRAM cells provide >70% less Isb and >40% speed gain over 28nm HK/MG as shown in Fig.10. The butterfly curves of the 0.07um² HD SRAM cell at different voltages are illustrated in Fig.11, where the Static Noise Margin (SNM) of 120mV at 0.6V is obtained. Write assist is validated with 128Mb HD SRAM test-chip with >300mV Vccmin reduction. Fig. 12a show 7-level Cu/low-k metal cross-section view of metal stacks having 1x pitch metal (M1 to M3) and 1.25x pitch metal (M4 and M5). The stacked via Rc is shown in Fig. 12b with good yield and tight distribution.

**Device and Interconnect Reliability**

Gate dielectric quality and process uniformity are keys to improve dielectric breakdown characteristics of 16nm FinFET. Both NMOS and PMOS TDDB are better than 28nm HK/MG planar devices, as illustrated in Fig. 13a and 13b, respectively, resulting from HK/MG process optimization that improves the gate dielectric quality and uniformity. Bias temperature instability (BTI) is challenging for FinFET, particularly PMOS, due to higher interface trap density at fin sidewall as reported in literature [4]. By careful gate stack process optimization to reduce the interface trap density, excellent BTI reliabilities are achieved. Fig. 14a and 14b show that PBTI is significantly improved as compared to 28nm HK/MG planar devices and NBTI is comparable. The 80nm pitch metal interconnects are developed as an additional low cost option for smaller circuit area and better routing flexibility. Decent interconnect reliability performance is demonstrated to assure its quality. Excellent EM performance of Vx/Mx & Vx/Mx+1 for 80nm pitch metal is shown in Fig. 15 as an example. Good interconnect thermal stability is illustrated in Fig. 16 with negligible resistance shift percentage of Kevin Rc structures having on-rule and wide metal. The TDDB lifetime for metal line-line and metal line-via is demonstrated with enough margins.

**Conclusion**

A highly manufacturable 16nm FinFET CMOS foundry technology featuring digital & analog functions, dense memory and MiM is presented. Fully functional 128Mb HD SRAM (with single fin) test-chip is demonstrated with high yield. Overall technology PPA yields >35% speed gain or >55% power reduction over our 28nm HK/MG technology with 2X logic density.

References


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<th>16nm Technology Features</th>
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<td>Process</td>
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<td>Analog</td>
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<th>28HK/MG</th>
<th>16FinFET</th>
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<tr>
<td>Normalized Power</td>
<td>0.2</td>
<td>1.2</td>
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<td>Normalized Speed</td>
<td>1.2</td>
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Fig. 2 16nm FinFET provides >35% speed gain or >55% power reduction over 28nm HK/MG planar

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<td>NOS at Vdd=0.75V</td>
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**Table. I Summary of 16nm FinFET key technology features**
Fig. 5 NMOS and PMOS Id-Vg characteristics of multi-Vt devices with Lg=30nm for uLVt/LVt and Lg=34nm for SVt.

Fig. 6(a) Better 1/f noise performance is illustrated in FinFET NMOS.

Fig. 6(b) Comparable 1/f noise performance is obtained in FinFET PMOS.

Fig. 7(a) NMOS mismatch improves by 36% over 28nm HK/MG planar.

Fig. 7(b) PMOS mismatch improves by 24% over 28nm HK/MG planar.

Fig. 8 FinFET devices show significant Gm/Gds and Gm/Id improvement over 28nm HK/MG planar.

Fig. 9 C-V characteristics of core and I/O NPoly/NWell varactors.

Fig. 10. SRAM C/I vs. Isb comparison between FinFET and HK/MG.
Fig. 11. Static noise margin of 0.07um² high density SRAM cell at 0.8V and 0.6V

Fig. 12 (a) Cross-section view of Cu/Low for 7-level metal, (b) Cumulative distribution of stacked via Rc resistance

Fig. 13(a) NMOS FinFET device shows better TDDB than 28HKMG

Fig. 13(b) PMOS FinFET device shows better TDDB than 28HKMG

Fig. 14(a) FinFET shows better PBTI than 28HKMG planar

Fig. 14(b) FinFET achieves comparable NBTI as 28HKMG planar

Fig. 15 Robust EM of Vx/Mx and Vx/Mx+1 for 80nm metal pitch

Fig. 16 Via resistance shifts of Kelvin structures with on-rule and wide metal (2um) after thermal stress for 500 hrs