A 2 dB NF, Fully Differential, Variable Gain, 900 MHz CMOS LNA

Enrico Sacchi¹, Ivan Bietti¹, Francesco Gatta², Francesco Svelto³ and Rinaldo Castello²

¹ "Studio di Microelettronica", STMicroelectronics, via Ferrata 1, 27100 Pavia, Italy;
² Department of Electronics, University of Pavia, via Ferrata 1, 27100 Pavia, Italy;
³ Department of Engineering, University of Bergamo, viale Marconi 5, Dalmine (BG), Italy.

Abstract

A fully differential 900 MHz CMOS LNA using, as input stage, nMOS and pMOS inductively degenerated pairs, in shunt configuration, achieves the following performance: 2 dB NF, 22 dB voltage gain, -3 dBm IIP3 with 8 mA current consumption. As additional feature this LNA has a variable gain. Measurements have been performed on packaged dies. No external components are used, except for an SMD inductor (used for tuning purposes), placed in series with the on-chip gate spiral inductor.

Introduction

CMOS RF building blocks (e.g. LNA, mixers, etc), achieving tough requirements such as specified by the most stringent standards (e.g. GSM and DCS-1800 systems), have been realized [1], [2]. Moreover, CMOS transceivers for more relaxed standards (e.g. wireless LANs) have been presented [3]. Nonetheless, to arrive at a monolithic CMOS solution meeting the specifications of future third generation systems, some issues still need to be addressed: first, the power consumption has to be lowered to be compatible with the requirements of longer battery life. Second, the system specifications have to be achieved using differential solutions. This is to insure an adequate rejection of the noise and of the interfering signals travelling through the common substrate.

In this paper, we propose a variable gain, fully differential 900 MHz CMOS LNA, achieving 2 dB NF, while drawing 8 mA. The input stage, which primarily determines the noise figure, makes use of inductively degenerated nMOS and pMOS pairs, in shunt configuration, to enable current reuse thereby saving power. In a 0.35 μm CMOS technology, this topology proves already to be advantageous over the traditional inductively degenerated nMOS pair. Furthermore, the proposed topology is expected to be more and more advantageous in further scaled technologies, where the difference in the cut-off frequencies of p and n devices will tend to decrease.

The noise figure is particularly low, considering that measured prototypes are packaged and all the inductors are realized as spiral inductors, except for an external inductor (in series with the gate inductor) used for tuning purposes.

LNA Design

A. Input Stage

The requirements set on the LNA input stage are: 50 Ω input matching, minimum noise contribution, maximum transconductance gain. Beside, the IIP3 of the LNA should be maximized.

It has been shown that the optimum solution that simultaneously fulfills all the above requirements is the inductively degenerated nMOS input stage shown in Fig. 1, in its differential form [4]. In fact, this topology allows to achieve a real input impedance (given by \( r_f \times L_s \), where \( r_f \) is the nMOS cutoff frequency) at the carrier frequency \( f_c \) (provided \( \omega_c = 1/\sqrt{(L_s + L_G)C_{GS}} \), where \( C_{GS} \) is the gate to source capacitance of the active devices). In other words, the series feedback allows the use of almost noiseless reactive elements to produce a real input impedance. This means that the noise is contributed, at least to first order, by the active devices only.

Fig. 1. The classical differential nMOS input stage.
for a given current consumption but also increases the sensitivity to external disturbances. In this design, we do not use transformers. This means that the input resistance has to be 50 Ω at the carrier frequency (fc = ωc/2π = 900 MHz).

The same trade-off exists between transconductance gain and biasing current, if the LNA is designed for minimum noise figure. In fact, by inspection of the circuit, the input stage transconductance (Gm), in matching conditions, is given by:

\[ G_m = \omega_r \frac{2 \omega_0 R_S}{2 \omega_0 R_S} \]  

in which \( R_S \) is the source resistance. The gate-to-drain overlap capacitance has been neglected to derive Eq. 1.

As a result, \( \omega_r \) is the only available design parameter to increase the input transconductance. The aspect ratio of the device is fixed to minimize the noise figure. Assuming, as an example, a 0.35 μm CMOS technology, 900 MHz carrier frequency, the optimum width is 600 μm. For a typical 4 mA current, biasing each device of the input pair, the \( \omega_r \) is 2π times 15 Grad/sec. This is far from the peak value (equal to 2π times 38 Grad/sec). This means that \( \omega_r \), and as a consequence the transconductance gain, can be increased at the expense of current consumption.

Finally, since the aspect ratio is set, also the overdrive voltage of the active devices, and then the linearity, is increased by increasing the current consumption.

Though beneficial for the noise figure, the transconductance gain and the linearity, the increase of the current consumption is in contrast with the requirements of a portable system. On the other hand, the same goal, i.e. improved performance in terms of gain, noise and linearity can be achieved by shunting an nMOS input stage with a pMOS one, without increasing the current consumption. To qualitatively understand the potential amount of this improvement, we assume, only for the sake of argument, that pMOS and nMOS devices have the same cut-off frequency. In this case, it is obvious that the new optimum device size for the two input differential pairs is half of that calculated for the simple nMOS pair. From this, it follows that the circuits of Fig. 2 are equivalent. This means that the transconductance of the shunt configuration, comprising an nMOS input stage together with a pMOS input stage, is \( \sqrt{2} \) times the transconductance of the nMOS only stage, for the same biasing current. From the noise standpoint, the short circuit output noise power spectral density of the shunt configuration is \( \sqrt{2} \) as much that of the nMOS only stage, biased at the same current level. However, the transconductance gain is also \( \sqrt{2} \) times higher.

As a result, the input referred noise power spectral density is \( 1/\sqrt{2} \) times in the shunt configuration than in the nMOS only stage. From the linearity standpoint, the IIP3 of the shunt configuration is \( \sqrt{2} \) times higher than that of the nMOS only stage. This can be intuitively understood considering that the input signal that appears across the gate source junction is the same in the two cases, but the overdrive voltage of the nMOS and pMOS devices, in the shunt configuration, is \( \sqrt{2} \) times as much because the active devices have half gate width and the same biasing current.

Actually, the assumption of equal cut-off frequency is not true, although technology scaling goes in the direction of reducing the difference between pMOS and nMOS cut-off frequencies. Specifically, for the 0.35 μm technology used, at the optimum bias point (from the noise point of view) and for a current of 8 mA differential, the ratio between \( \omega_{r,p} \) and \( \omega_{r,n} \) is 2.5. As a result the design for minimum noise requires different gate width for pMOS and nMOS devices also because they feature different thermal and induced gate noise coefficients. In fact, with the same dimensions, the contribution to the NF coming from nMOS devices would be higher than that from pMOS one. One way to reduce the nMOS contribution is to increase its synthesized resistance at resonance, together with decreasing the pMOS synthesized resistance, since the parallel of the two has to be equal to 50 Ω. Following this idea simulations were performed for the two possible configurations (nMOS only and p-n shunted), relatively to a 0.35 μm and 0.18 μm CMOS technology, using the Philips MM9 device models. The results are summarized in Table I. Notice that the actual transconductance is slightly lower than in the nMOS only configuration. Nevertheless the IIP3 is proportionally higher.

### B. Variable Gain and Output Stage

The large amplitude range of signals, received in antenna in wireless communications systems, requires variable gain stages. This is to enhance the signal to noise ratio, in presence of minimum amplitude signals, while not saturating the last stages of the receiver, in presence of maximum amplitude signals.

The LNA, proposed here, features a variable gain, realized by a differential pair, which steers the input stage cur-

### TABLE I

COMPARISON BETWEEN SIMULATED OPTIMUM nMOS AND p-n MOS DIFFERENTIAL LNA (f = 900 MHz)

<table>
<thead>
<tr>
<th>Type</th>
<th>Tech.</th>
<th>Gm</th>
<th>noise</th>
<th>IIP3</th>
<th>NF</th>
</tr>
</thead>
<tbody>
<tr>
<td>nMOS</td>
<td>0.35 μm</td>
<td>175</td>
<td>5.46 x 10^-19</td>
<td>-7</td>
<td>2.2</td>
</tr>
<tr>
<td>p-n</td>
<td>0.35 μm</td>
<td>2.5</td>
<td>158</td>
<td>3.97 x 10^-19</td>
<td>+1</td>
</tr>
<tr>
<td>nMOS</td>
<td>0.18 μm</td>
<td>338</td>
<td>3.47 x 10^-19</td>
<td>-5</td>
<td>1.5</td>
</tr>
<tr>
<td>p-n</td>
<td>0.18 μm</td>
<td>1.7</td>
<td>285</td>
<td>2.4 x 10^-19</td>
<td>+2.6</td>
</tr>
</tbody>
</table>

Fig. 2. Equivalence between p-n input stage and classic nMOS input stage (single-ended).
rent signal either to the LC output load or to VDD. Fig. 3 shows the LNA complete schematic. Notice that, in the high gain mode, the on transistors of the differential pairs (M6 and M7) behave as the common gate of the input cascode structure. This is highly desirable to decouple the input from the output stage, preventing thus far possible common mode oscillations.

**Experimental Results**

The LNA of Fig. 3 has been realized in a 0.35 μm CMOS RF technology. All the inductors are integrated spiral inductors. The thick, top metal layer has been used to realize the spiral of metal. The quality factor of the inductors is 7 at 900 MHz.

It is worthwhile to underline that the gate inductance is 10 nH, approximately half of which obtained with an integrated spiral inductor (LG). This gives a noise penalty, but goes in the direction of complete integration. On the other hand, the external inductor is meant to tune the input stage.

To drive the 50 Ω Network Analyzer input impedance, two output buffers (not shown for the sake of simplicity) have been added. Prototypes have been encapsulated in a SO20 plastic package.

Fig. 4 shows the voltage gain at core output measured versus frequency. In particular curve a) represents a measurement in the following conditions: VDD = 2.7 V, I = 8 mA, high gain mode. The peak value is 22 dB. The frequency of the measured peak (732 MHz) is different from the designed one (900 MHz). This is due to a large capacitive parasitic in the output load, caused by too large metalizations connecting the inductor to the capacitor. This was verified performing a post-layout simulation, unfortunately after silicon submission. Curve b) shows the voltage gain when the differential pairs (M5, M6) and (M7, M8) are balanced, i.e. only half of the signal is injected into the load. A 6 dB gain reduction, in the overall frequency range, is found. Finally, it has been verified, experimentally, that for a bias of the gain control voltage adequately high, the output signal disappears and no gain is realized.

Fig. 5 shows the post-layout simulated and measured noise figure. The operating conditions are: VDD = 2.7 V, I = 8 mA, high gain mode. An excellent agreement is evident. The minimum measured value is 2 dB. This is also in agreement with the results of table I, predicting a 1.7 dB NF for the input stage, if we take into account the noise due to the gate spiral inductors.

The measured noise figure is unchanged even if the voltage supply is lowered to 2 V.

If the pMOS section is switched-off, the noise figure raises to 2.8 dB. This is again in very good agreement with simulations. Two reasons determine the noise figure increase: first the input stage noise figure increases, and second the noise contributed by the current switch and by the output stage is higher due to the reduced transconductance. As highlighted above, the increase of the current consumption determines a reduction in the noise figure. The current...
TABLE II
A COMPARISON BETWEEN LNAs PRESENTED IN LITERATURE AND THAT HERE DESCRIBED

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>Single-ended</td>
<td>0.8 μm</td>
<td>0.9</td>
<td>1.5</td>
<td>5</td>
<td>12.4</td>
<td>-1.9</td>
<td>packaged, off-chip tuning</td>
</tr>
<tr>
<td>[5]</td>
<td>Single-ended</td>
<td>0.25 μm</td>
<td>0.9</td>
<td>1.6</td>
<td>4</td>
<td>16.4</td>
<td>-7.3</td>
<td>unpackaged, off-chip tuning</td>
</tr>
<tr>
<td>[6]</td>
<td>Differential</td>
<td>0.5 μm</td>
<td>1.5</td>
<td>2.4</td>
<td>5</td>
<td>16 *</td>
<td>-9</td>
<td>off-chip tuning</td>
</tr>
<tr>
<td>This work</td>
<td>Differential</td>
<td>0.35 μm</td>
<td>0.9</td>
<td>2</td>
<td>8</td>
<td>22 *</td>
<td>-3</td>
<td>packaged, on/off-chip tuning</td>
</tr>
</tbody>
</table>

* Voltage gain at core output

Fig. 5. Comparison between measured and simulated Noise Figure versus frequency.

Fig. 6. Measured IIP3.

**Conclusions**

The proposed LNA, in which the input stage is realized connecting inductively degenerated pMOS and nMOS pairs, gives a very low noise figure at low current consumption. This should improve in deeper scaled technologies. Notice that the very good measured results were obtained with a fully differential version of the LNA and the measured prototypes were packaged. Table II shows how these results compare with state of the art of integrated CMOS LNAs. The current I is the current consumed by the LNA input stage. The gain, relative to [1] and [5], is a power gain, whereas the gain, relative to [6] and this work, is the voltage gain at the core output.

**Acknowledgement**

This work has been performed in the framework of the ESPRIT project CRAFT.

**References**


