Inverse Watkins–Johnson Topology-Based Inverter

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Abstract—A Z-source inverter (ZSI) uses an L–C impedance network between the source and the voltage source inverter (VSI). It has the property of stepping down or stepping up the input voltage, as a result, the output can be either higher or lower than the input voltage as per requirement. This topology also possesses robust electromagnetic interference noise immunity, which is achieved by allowing shoot through of the inverter leg switches. This letter proposes an inverter circuit based on the inverse Watkins–Johnson (IWJ) topology that can achieve similar advantages as that of a ZSI. The proposed circuit requires two switches and one pair of an LC filter apart from the VSI. The systematic development of this inverter topology is described starting from the basic IWJ circuit. Steady-state analysis and implementation of the proposed topology are also described. The pulse width modulation control strategy of the inverter is explained. An experimental prototype is used to validate the proposed circuit.

Index Terms—Continuous conduction mode, boost converter, voltage source inverter (VSI), Watkins–Johnson converter.

I. INTRODUCTION

THE use of Z-source network enables an inverter to have voltages higher or lower than the input voltage. The Z-source inverter (ZSI) consists of two switches and an L–C network connected in form of an “X,” cascaded to a voltage source inverter (VSI), as shown in Fig. 1. The switch closer to the input voltage is realized using a diode for unidirectional power flow application, e.g., fuel cells and solar panel. The second switch S is connected between $V_{g1}$ and $V_{o2}$, and is a part of the inverter switching network. This is realized by turning ON the switches of the same leg $S_a$ and $S_g$ at the same time. This is perceived as an advantage as it enables a shoot-through state for the inverter legs [1], [2]. By controlling the simultaneous turn-ON time of ($S_a$ and $S_g$), ideally, the inverter input can be varied to any level above the input $V_g$. Therefore, the output of the inverter can be either higher or lower than $V_g$. The shoot-through state in the inverter improves the electromagnetic interference (EMI) tolerance of the inverter and makes it more reliable. Note that the inverter input ($V_{o1}$–$V_{o2}$) is a switched waveform and not a constant as is the case for a conventional VSI.

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Normally, the two L–C filters of the Z-source network are chosen to be symmetrical. If the LC network is nonsymmetrical, it leads to unequal pole-zero pairs and creation of complex right half plane (RHP) zero pairs at low frequencies [3]. Based on the preceding discussion, the ZSI properties are summarized as follows.

1) It produces an inverter output voltage higher or lower than the input voltage $V_g$.
2) It allows shoot through of the inverter switches leading to better EMI noise tolerance.

This letter describes an inverse Watkins–Johnson (IWJ)-based inverter topology that has an operational behavior similar to a ZSI. This new inverter topology is referred to as the switched-boost inverter. The next section reviews the fundamental operation of an IWJ converter. The development of switched boost inverter (SBI) from an IWJ topology and its performance comparison with VSI and ZSI are described in Section III followed by its pulse width modulation (PWM) control strategy. Section V provides experimental verifications to validate the proposed circuits. In this letter, an upper-case symbol refers to the steady-state quantity, upper case with a hat (\(^\hat{\cdot}\)) refers to the peak value, and lower case symbol refers to instantaneous quantity.

II. REVIEW OF IWJ CONVERTER

The schematic of an IWJ-based converter is shown in Fig. 2(a) and its steady-state transfer characteristic is shown in Fig. 2(b) [4], [5]. The equivalent circuit configuration during $D$ and $D'$ are shown in Fig. 2(c) and (d), respectively. In the $D$ interval (position 1), the inductor is connected between the input and the output. During $D'$ interval (position 0), the inductor is connected between the output and the ground. Using volt-second balance, the relationship between the output and the input under the steady state is given in the following equation, which is in fact plotted in Fig. 2(b):

$$M(D) = \frac{V_{o_{IWJ}}}{V_g} = \left( \frac{D}{D - D'} \right).$$  (1)
Fig. 2. (a) IWJ converter, (b) conversion ratio of an IWJ converter, (c) IWJ in interval $D.T_S$, and (d) IWJ in interval $D'.T_S$.

Fig. 3. Development of the inverter topology with Z-source property using an IWJ topology. (a) IWJ topology. (b) CIWJ topology. (c) CIWJ topology redrawn. (d) Shifting the load from constant voltage terminal to the switching terminal to obtain switched-boost converter.

The output is negative below $D = 0.5$ and positive above $D = 0.5$. Ideally, the magnitude of the output is very high in the vicinity of $D = 0.5$.

III. DEVELOPMENT OF IWJ-BASED INVERTER

A. Circuit Development

Fig. 3(a) redraws the IWJ converter. Interchanging the $D$ (position 1) and $D'$ (position 0) of IWJ leads to Fig. 3(b). This configuration is named as the complementary IWJ (CIWJ) in this letter. Note that this interchange has no impact on the states of the converter. However, as far as implementation is concerned this will imply that the controlled switch and diode of CIWJ and IWJ are interchanged. The CIWJ is redrawn in Fig. 3(c). Taking a closer look at the circuit, it can be observed that similar to Z-source converter, during $D$ (position 1) interval, the inductor and the capacitor are connected in parallel. During $D'$ (position 0) interval, the inductor is connected between the input voltage and the capacitor.

The load can be either connected across the capacitor or the switching terminal as shown in Fig. 3(c) and (d), respectively.

Fig. 4. Implementation of switched-boost topology, critical waveforms, and conversion ratio.

The implementation in Fig. 3(d) is called the SBI topology. The resistor $R_o$ may be replaced by an H-bridge inverter. Note that Z-source topology can also have these two variations in load placement, as given in [6]. It is interesting to note that the IWJ converter cannot be used to realize an inverter due to following reasons. 1) There is a diode in parallel with the resistor (or inverter), which makes it impossible to locate the inverter across the diode terminals. 2) SBI has the advantage of input diode blocking making it suitable for fuel-cell- or solar-cell-based systems. This advantage will be lost in an IWJ-based inverter.

B. Steady-State Characteristic

Continuous conduction mode is assumed in the following analysis. Fig. 4(a) shows the implementation of switched boost inverter that is shown in Fig. 3(d). Fig. 4(b) shows the critical switching waveforms of the switched-boost topology. During $D$ interval [see position 1 in Fig. 3(d)], $S_1$ and $S$ are turned ON at the same time, which connects $L$ and $C$ in parallel and charges the inductor. During the $D'$ interval [see position 0 in Fig. 3(d)], $S$ is turned OFF, which forces $D_1$ and $D_2$ to turn-ON enabling the inductor to discharge into the load (inverter). $V_{S2}$ becomes equal to $V_C$ during this interval. Replacing $D$ with $D'$ in (1), the transfer characteristic of CIWJ is given by the following equation:

$$M(D) = \frac{V_{O_{CIWJ}}(=V_C)}{V_g} = \left( \frac{D'}{D' - D} \right)$$ (2)

where $V_{O_{CIWJ}}$ is the voltage across the capacitor.

The aforementioned characteristic is plotted in Fig. 4(c). Note that this transfer characteristic is same as that exhibited by a Z-source converter. Near $D = 0.5$, the steady-state gain is very high. The inverter is connected between $V_{S2}$ and ground. A shoot-through interval is required, similar to a ZSI. It is worth noting that the proposed inverter works similar to a conventional
TABLE I
COMPARISON OF VARIOUS INVERTERS

<table>
<thead>
<tr>
<th>Particular</th>
<th>SBI</th>
<th>ZSI</th>
<th>VSI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Converter type</td>
<td>Buck</td>
<td>Buck</td>
<td>Buck</td>
</tr>
<tr>
<td></td>
<td>or Boost</td>
<td>or Boost</td>
<td></td>
</tr>
<tr>
<td>Number of passive components</td>
<td>4</td>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>Switches</td>
<td>Active</td>
<td>Passive</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1+4=5</td>
<td>0+4=4</td>
<td>4</td>
</tr>
<tr>
<td>Shoot-through tolerance</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

Fig. 5. Switching state comparison between SBI and ZSI.

inverter and also has the ZSI properties in sense that one of the VSI inputs is always connected to the supply ground. In case of a ZSI, the VSI inputs are floating.

It is interesting to note that, the conventional mode of operation of the inverter is at $D < 0.5$. When the inverter is operated with $D > 0.5$, the capacitor voltage $V_C$ is negative. The SBI topology as shown in Fig. 4(a) will not operate properly under this condition. As the output voltage before startup is predefined to $V_g$, the circuit fails to achieve the steady state. In order to enable the operation of SBI with $D > 0.5$, the diodes $D_1$ and $D_2$ must be replaced by controlled switches. The voltage stress across the switches under this mode of operation is higher compared to operation under $D < 0.5$.

C. Performance Comparison

The major differences between the SBI, ZSI, and VSI are tabulated in Table I. As pointed out earlier, SBI is an active implementation of ZSI (with symmetrical LC network) because the converter states during the switching intervals remain unchanged. In comparison, the SBI requires more active components and less passive components for implementation.

Fig. 5 shows the comparison between ZSI and SBI during a switching cycle. As far as the input impedance seen from the H-bridge inverter is concerned, the state equations are identical for both the topologies, leading to an equal low-frequency input impedance. The peak voltage across $S$ is $(V_g - V_C)$ and across $D$ is $V_C$ in case of the SBI. Note that this topology requires one more controlled switch $S$ compared to a ZSI. The advantage of the proposed IWJ-based inverter is that for the same input voltage, capacitor voltage, output voltage, and output power, it operates at lower peak inverter input voltage. Therefore, there is reduced voltage stress and higher current requirement of the inverter switches compared to a ZSI. The switch utilization ratios [7] are nearly equal if the input voltage, capacitor voltage, output voltage, and output power are the same for the ZSI and SBI.

In a traditional VSI, if there is a shoot through in the inverter leg due to EMI noise, inverter switches can damage itself due to high short-circuit current. In ZSI, if there is a shoot through due to EMI noise, the shoot-through current is limited by the impedance network. Similarly, in a SBI, if there is a shoot through due to EMI noise, the shoot-through current is limited by the inductor $L$ and consequently the inverter switches will not be damaged. Therefore, it can be observed that SBI exhibits better EMI noise immunity compared to traditional VSI, similar to a ZSI.

D. Failure Mode

The proposed converter also has high input impedance during normal operation. Referring to Fig. 5, during $D^*$-interval, the inductor is in series with the source. During the $D$-interval, the input diode $D_1$ is OFF as $V_c$ is higher than $V_g$. The source is, thus, completely isolated.

There remains the failure mode in which the switch $S$ becomes short, permanently. In this case, input diode $D$ is OFF till $V_c$ is larger than $V_g$, keeping the source isolated. After this $V_C$ is clamped to $V_g$ and the inductor $L$ remains in series with $V_g$. As the H-bridge operates with $L$ in series with its input, the output current is limited. If the inverter switches are turned OFF by a protection circuit, the inductor current can freewheel through the diode $D_2$ and $S$ till it safely decays to zero.

There is a possibility, though very rare, that both input diode $D$ and the switch $S$ fail simultaneously. In such a case, the capacitor will discharge rapidly to the voltage $V_g$. But the excess stored energy is limited and the resulting current peak will be of small duration. The inductor $L$ will remain in series with the source $V_g$ in this case also. Thus, the proposed inverter is capable of providing high input impedance under normal as well as fault condition.

IV. SWITCHED-BOOST INVERTER IMPLEMENTATION AND PWM CONTROL STRATEGY

The conceptual circuit in Fig. 4(a) can be implemented using power devices, as shown in Fig. 6(a). A separate switch $S_1$ is not required as it can be realized by turning ON the inverter leg switches $S_1$–$S_2$ or $S_3$–$S_4$, simultaneously. Note that the switch $S$ has a floating gate. This switch can either be turned-ON using a boot-strap gate driver circuit or a floating driver (e.g., driver with optoisolator). Nevertheless, the gate-drive supply has to be floating.

Modifications are done to the conventional unipolar PWM control to make it suitable for SBI. The modification incorporates a shoot-through interval be inserted as part of the PWM control. Fig. 6(b) shows the control circuit to implement the proposed PWM scheme, and Fig. 7 shows the signals required and generated by this control circuit. As shown, the gate signals $G_{S_{N}}$ ($N = 1$–4) are generated by comparing the reference signal $Ref_{S_{N}}$ ($N = 1$–4) with a triangular carrier signal $v_{tri}(t)$. The signals $S_a$ and $S_b$ are two shoot-through periods derived from $G_{S_1}$–$G_{S_2}$ and $G_{S_3}$–$G_{S_4}$, respectively. The gate signal $G_c$ is then
obtained by logically adding these two individual shoot-through periods \( S_a \) and \( S_b \).

To determine a mathematical relation between the shoot-through duty ratio \( D \) and the offset \( v_{off} \), consider Fig. 7(c), from which it can be deduced

\[
\begin{align*}
\hat{v}_{tri}(t) &= \left| \hat{v}_{tri} \right| \left( \frac{t}{T_S/4} - \frac{1}{2} \right) & \text{if } 0 < t < \frac{T_S}{2} \\
&= \left| \hat{v}_{tri} \right| \left( \frac{1}{2} - \frac{t}{T_S} \right) & \text{if } \frac{T_S}{2} < t < T_S
\end{align*}
\]

\[
v_{tri}(t) = v_m(t) \quad \text{if } t_1 < t < t_2 - t_1
\]

Now, using (3) and (4), the expressions for \( t_1 \) and \( t_2 \) can be written as

\[
t_1 = \frac{T_S}{4} \left( 1 - \frac{v_m(t_1) + v_{off}}{\hat{v}_{tri}} \right) \quad \text{and} \quad t_2 = \frac{T_S}{4} \left( 1 - \frac{v_m(t_2) + v_{off}}{\hat{v}_{tri}} \right)
\]

Substituting \( t_1 \) and \( t_2 \) in (5), we get

\[
\frac{v_m(t_1) - v_m(t_2) + v_{off}}{\hat{v}_{tri}} = D.
\]

Since the frequency of the carrier signal is much higher than the frequency of the modulation signal, it can be assumed that \( v_m(t_1) = v_m(t_2) \). Using this relation in (6), the relation between \( v_{off} \) and \( D \) can be obtained as

\[
v_{off} = D \cdot \hat{v}_{tri}.
\]

Also, for the inverter to operate in linear modulation range, the value of the reference signal, generated using control schematic of Fig. 6(b), should always be less than the peak value of carrier signal \( \hat{v}_{tri} \) or

\[
\max (v_m(t) + v_{off}) < \hat{v}_{tri} \Rightarrow m \cdot \hat{v}_{tri} + D \cdot \hat{v}_{tri} < 1 \\
\Rightarrow m + D < 1.
\]

So at any time, the sum of modulation index and shoot-through duty ratio should be less than unity.

V. EXPERIMENTAL RESULTS

A prototype is built to test the proposed SBI and its PWM control. The design parameters and the list of semiconductor components used for the prototype are given in Tables II and III, respectively.

Fig. 8(a) shows the PWM signals of the gates. The converter switch nodes with respect to the PWM signal are shown in Fig. 8(b). \( V_2 \) is the input to the VSI. Fig. 8(c) shows the overall SBI output, input voltage, and the capacitor voltages. With a 53-V input, the capacitor voltage is 163 V that is used to derive a 140 V (pk–pk) inverter output. As per the design criterion in (8), the modulation index of the inverter is around 0.42 for this design.

Fig. 9 shows the converter startup waveform where the SBI and the H-bridge are turned at the same time to provide discharge path for the dc capacitor. The dc capacitor voltage starts from \( V_g \) reaches the steady state after 20 ms. The inrush current at startup is regulated by the ac load (output capacitor \( C_f \)) and the current required by the capacitor \( V_c \) to charge.

The harmonic spectrum of inverter’s output voltage \( v_{ab} \) with \( D = 0.4, M = 0.5 \) is plotted in Fig. 10. Note that the values of \( D \) and \( M \) are satisfying the inequality given in (8). Table IV compares the dominant harmonics present at the output of the SBI and a traditional VSI with conventional unipolar sine-triangle PWM [7]. It can be concluded from these results that, with the proposed PWM technique, the shoot-through state of the SBI will have no effect on the harmonic spectrum of its output voltage \( v_{ab} \), provided that the sum of the shoot-through duty ratio and modulation index is less than unity.
Fig. 7. (a) PWM inputs. (b) fundamental waveforms. (c) Close-up view of generation of the shoot-through interval.

Fig. 8. Waveforms of the SBI (see in Fig. 6) (a) PWM control signals. (b) Switching waveforms of the converter. (c) Operation of the inverter circuit.

Fig. 9. Converter start-up waveform.

Fig. 10. Harmonic spectrum at the output of the inverter $v_{ab}$.

TABLE IV
COMPARISON OF DOMINANT HARMONICS

<table>
<thead>
<tr>
<th>Harmonic Number (m)</th>
<th>Frequency (Hz)</th>
<th>Normalized Magnitude ($m_n/200$)</th>
<th>SBI (Experimental)</th>
<th>VSI (Theoretical)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>50</td>
<td>0.47</td>
<td>0.5</td>
<td></td>
</tr>
<tr>
<td>2m±1</td>
<td>20000 ± 50</td>
<td>0.36</td>
<td>0.361</td>
<td></td>
</tr>
<tr>
<td>2m+3</td>
<td>20000 ± 50</td>
<td>0.07</td>
<td>0.044</td>
<td></td>
</tr>
<tr>
<td>4m±1</td>
<td>40000 ± 50</td>
<td>0.1</td>
<td>0.091</td>
<td></td>
</tr>
<tr>
<td>4m+3</td>
<td>40000 ± 50</td>
<td>0.07</td>
<td>0.107</td>
<td></td>
</tr>
</tbody>
</table>

VI. CONCLUSION

This letter proposes the development of an IWJ topology-based inverter. The proposed inverter is called the SBI and it exhibits properties similar to a ZSI. Namely, it has the property of a buck and boost topology and it allows shoot through of inverter leg switches to improve EMI immunity of the inverter. The systematic development of the inverter is presented. The steady-state analysis of the inverter and its PWM control strategy are also presented. The proposed topology and its control are experimentally validated.

REFERENCES
