The Simulation and Design of PSFB ZVS DC-DC Converter Based on Saber

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Abstract—Firstly, the operation principles of a conventional phase-shifted full-bridge (PSFB) zero voltage switching (ZVS) DC-DC converter is briefly introduced. PI control strategy used in voltage loop and current loop is also presented. Secondly, a corresponding simulation model of PSFB based on Saber is built up. The simulation results show a constant output voltage. Phase-shifted and ZVS state have been realized in the simulation results, which verifies the effectiveness of the control system. Finally, the test results of a Prototype based on UCD3138 are also demonstrated in the text.

Keywords: PSFB DC-DC Converter, ZVS, Saber simulation

I. INTRODUCTION

In order to reduce switching loss and increase power density in DC-DC converters at high power and high frequency, many literatures have proposed new techniques[1-3]. For medium-to-high power applications, the conventional PSFB DC-DC converter has drawn more attention in recent decades due to its advantages: high conversion efficiency, high power density, and low electromagnetic interference (EMI)[4, 5].

Using the switch tube junction capacitance and leakage inductance of high frequency transformer as the resonant component, the MOSFET turns on with zero voltage transition.

II. OPERATION PRINCIPLES OF PSFB AND ITS CONTROL

BLOCK DIAGRAM

PSFB DC-DC converter circuit is shown in Fig.1. To simplify the steadystate analysis of the circuit during one switching cycle, the following assumptions are made[6]:

1) the input voltageVin is constant;
2) diodes are ideal devices;
3) the blocking capacitorC1 is large enough to be neglected at high-frequency operation.

Fig.2 is the working process of PSFB. Black lines are the current flow in the figure.

Stage 1 (Fig.2 (a)): At the beginning of this stage, Q1 and Q4 are conducting. Input voltageVin is applied to the transformer’s primary and power is transferred to the output. Output current flows through the diodeD2.

Stage 2 (Fig.2 (b)): Turn off Q1, then the current in Q1 transfers to the capacitorsC1 and C2, at the same timeC1 charges andC2 discharges. Due to the low value ofC1, C2 in the circuit, the process of charging and discharging is quickly. CurrentI5 during this stage can be approximately considered as a constant value.

Stage 3 (Fig.2 (c)): After a full discharge ofC2, UO2=0 andD2 will conduct, which prepares for the goal thatQ2 turns on at zero voltage. Because theQ4 andD2 turn on at the same time, UAB=0 and the inverter bridge generates internal circulation, resulting in the stop of supply from DC power to the inverter. The voltage of output filter inductorL2 is equal to the value of the load voltage on the contrary, and energy stored in the filter inductor will release through the circuit consisted of the load andD2.

Stage 4 (Fig.2 (d)): Turn offQ4, thenC3 begins to discharge. UAB=—UO4, as UO4 rises, UAB negatively grows. Based on the homonymous port of high frequency transformer, D1 will turn on in the rectifier circuit. Because the current in the transformer can not abrupt change, in other words, current in theD1 cannot go down immediately, the state that theD1 andD2 conduct at the same time appears.

Stage 5 (Fig.2 (e)): After C4 has recharged andC3 has discharged, the gate voltageVQ3 ofQ3 is high. However, because the currentI5 flowing through the primary side of high frequency transformer is still positive, theD3 turns on andQ3 is still in the blocking state. There is not substantive change in the deputy side of the transformer, except that the currentI3 continues to decline and the currentI4 continues to rise untilI3=0, whereI3=I4.

Stage 6 (Fig.2 (f)): CurrentI5 inverts and increases. Q2 andQ3 achieve zero voltage conduction. I3 continues to decrease whereasI4 continues to increase untilI3 is zero.

After that, Q2 is turned off, and the other half cycle of DC-DC converter begins. It is similar to the above half cycle.

Fig. 1. PSFB DC-DC converter
PI control strategy is used in outer voltage loop and inner current loop. The difference between output voltage \( V_o \) and the given reference voltage is taken as the input of the outer loop. Whereas the output of outer loop is used as the reference of inner loop. The difference between it and the sampled output current is taken for the input of the inner loop. Its output, known as the angle \( \theta \), controls the pulses that drive the MOSFET\(^7\).

![Control block of the converter](image)

**Fig. 3.** Control block of the converter

![Operation stages](image)

**Fig. 2.** Operation stages
III. PSFB SIMULATION BASED ON SABER AND ITS PROTOTYPE

Saber which can simulate both analog and digital integrated circuits is one of the most popular and powerful electronic design automatic (EDA) software. It has a large common model base with more precise models for the specific types of components. What’s more, it has open interface and secondary development can be made on it\(^9\).

The simulation results are as follows:

\[ \text{Fig. 4. MOSFET driving waveforms PWM} \]

Waveforms in Fig.4 are added to gates of the four MOSFETs to drive them. Phase-shift angle equals to the difference between the axis \( x=0.0988 \) and the axis \( x=0.098804 \) in the figure. Dead time is from the axis \( x=0.098755 \) to the axis \( x=0.098759 \).

\[ \text{Fig. 5. The procedure of ZVS} \]

Fig.5 is the implementation of soft-switching process. When the difference voltage between drain and source of a MOS is equal to zero, the drive signal of gate turned to high level, contributing to the implement of zero voltage opening procedure of the tube. When the driving signal is withdrew, the difference voltage between drain and source of the MOS begins to increase due to the recharging of its capacitor.

\[ \text{Fig. 6. Input voltage and output voltage} \]

Fig.6 shows the input voltage and output voltage in the PSFB simulation.

Prototype and experiment results are as follows:

\[ \text{Fig. 7. Prototype and test equipments} \]

\[ \text{Fig. 8. PWM waveforms generated by IC} \]

Fig.8 is PWM diagram generated by IC. Due to the lack of experience in PCB board distribution, the PWM waveforms get some interference when it is transferred from the control circuit to the main circuit. The dead time is 240ns and the frequency is 140KHz.
Fig. 9: Two drive signals of one-leg

Fig. 9 is the drive signals added to the two tubes of one-leg. Zoom in, the two tubes are not at the risk of direct conduction in the dead time. But the glitch is large.

Under condition of no load, with the input voltage up to 390V, the prototype output voltage waveform of jagged amplitude up to 10V.

IV. CONCLUSION

In this paper, the operation principle of PSFB ZVS DC-DC converter has been analysed. The implementation of phase-shifted and ZVS in the PSFB ZVS DC-DC converter simulation based on Saber has been showed. What’s more, it also presents the test results of PSFB ZVS DC-DC converter prototype. Due to the lack of experience and the limit of time, the preset target of PSFB ZVS DC-DC converter prototype that inputs 400V and outputs constant 12V fails to be met. In the following, the hardware circuit will continue to be optimized, and its results will be released in the follow-up.

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