Bridged-T Coil for Miniature Dual-Band Branch-Line Coupler and Power Divider Designs

Wei-Ting Fang, Student Member, IEEE, En-Wei Chang, and Yo-Shen Lin, Senior Member, IEEE

Abstract—In this paper, a new design method for bridged-T coil (BTC) is proposed such that it can be made equivalent to two different transmission line sections at two different frequencies. In this way, on-chip dual-band branch-line coupler and dual-band power divider designs with very compact circuit sizes can be made possible through the use of BTCs. Specifically, the proposed 2.45/5.8-GHz dual-band branch-line coupler realized using the integrated passive device (IPD) process features a compact circuit size of only 2.8 mm × 1.4 mm while the proposed 2.4/5.5-GHz dual-band power divider in IPD exhibits a very small circuit size of only 1.8 mm × 1.7 mm. To the best of our knowledge, the proposed dual-band branch-line coupler is the smallest one ever reported while the circuit size of the proposed dual-band power divider is comparable to the smallest in the literature.

Index Terms—Branch-line coupler, bridged-T coil (BTC), dual band, hybrid coupler, integrated passive device (IPD), power divider.

I. INTRODUCTION

MODERN wireless communication systems are required to operate at several frequency bands and work across different communication standards. This much increases the complexity of the RF front-end circuitry. To reduce the system complexity and circuit size as well as cut down the cost, there have been rapid developments of multiband circuit components and subsystems in the past decade. Especially, various dual-band microwave passive component designs have been proposed in these years. In addition to numerous dual-band microwave filter designs that can be found in the literature, the designs of dual-band three- and four-port microwave passive circuits, e.g., power divider and hybrid coupler, have also gained substantial research interest recently.

Branch-line coupler is a key building block in many microwave systems. Several approaches have been proposed for the realization of dual-band branch-line coupler designs [1]–[19]. First, it can be obtained by replacing the quarter-wavelength (λ/4) lines in a conventional branch-line coupler with equivalent dual-band λ/4 transformers, which can be realized using either the composite right-/left-handed transmission line [1], the π-type dual-band λ/4 transformer in [2]–[5], or the T-type stub-loaded transmission line in [6]–[8]. Another popular approach for dual-band branch-line coupler design is by introducing additional transmission line sections through either the three-branch-line design [9] or the port extension technique [10] so as to provide additional design freedom and allow the synthesis of a dual-band frequency response. On the other hand, the cross-coupled branch-line coupler in [11] attains the dual-band capability with the additional cross-coupling branches. Coupled lines [12], [13] and rectangular [14] or circular patches [15] have also been employed in the design of dual-band branch-line couplers. In addition, compact dual-band branch-line couplers based on the low-temperature co-fired ceramic (LTCC) technology [16], meandered lines [17], dual transmission lines [18], or the coupled-resonator technique [19] have also been introduced recently to achieve a reduction in circuit size.

Power divider is also widely used in microwave circuit and system designs. Extension of the conventional Wilkinson power divider to a dual-band one has also been approached by many researchers. In [20], two-section transformers [21] are employed to replace the λ/4 lines in a conventional Wilkinson power divider to achieve a dual-band frequency response. Modified designs with additional lumped [22], [23] or distributed elements [24] are then proposed to achieve better performance. In [25], a new dual-band power divider with more realistic line impedances and wider ranges of frequency ratio comparing with [24] is presented with closed-form design equations, while a similar design is reported later in [26]. Just like many dual-band branch-line coupler designs, dual-band λ/4 transformers based on T-type stub-loaded transmission lines [27], [28], composite right-/left-handed transmission lines [29], or the lumped-distributed structures in [30]–[32] have also been used to achieve dual-band power divider designs. Additional transmission line [33] or coupled-line [34] sections can also be introduced to the input or output of a conventional Wilkinson power divider to allow the synthesis of a dual-band frequency response. In [35]–[37], coupled-lines are used to realize dual-band Wilkinson power dividers. In [38], the design of the two-section power divider with two absorption resistors is generalized to achieve the desired dual-band frequency characteristics. In addition to the Wilkinson power divider-based designs mentioned above, dual-band Gysel power divider designs have also been reported in [39]–[42]. Moreover, compact dual-band power divider designs based on the LTCC technology [43] or lumped elements [44], [45] have also been reported to largely reduce the circuit size.

Despite the large number of different approaches for dual-band branch-line coupler and power divider designs that have
been proposed in the literature, the common drawback of almost all conventional designs is the large circuit size. Considering the fact that most dual-band wireless communication systems nowadays work below 6 GHz, the large circuit size of conventional dual-band branch-line coupler/power divider designs prevents the use of them in mobile terminals. In our previous works [46]–[53], the bridged-T coil (BTC) [54] in Fig. 1(a) is utilized to realize various microwave passive components with very compact circuit sizes including power dividers [46]–[49] and branch-line couplers [50]–[53]. In this paper, through a simple modification, the BTC can be made equivalent to two different transmission lines at two different frequencies (i.e., \( f_a \) and \( f_b \)), as illustrated in Fig. 1(b). It can then be used to realize various transmission line-based microwave circuits to achieve the desired dual-band frequency characteristic with very compact circuit sizes. As a demonstration, the designs of miniature dual-band branch-line coupler and dual-band power divider will be proposed in this paper. The dual-band design of BTC will be presented in Section II. Design examples on miniature dual-band branch-line coupler and power divider will be given in Sections III and IV, respectively. Finally, a brief conclusion will be drawn in Section V.

II. DUAL-BAND DESIGN OF BTC

Fig. 1(a) shows the basic circuit structure of the conventional BTC [54]. It can be designed with a nearly all-pass response, so it is regarded as a wideband lumped-element equivalent of transmission line as illustrated in Fig. 1(a). Given the Z- and Y-parameters of the required transmission line at two frequencies of interest (i.e., \( f_a \) and \( f_b \)), the corresponding L and C values of the BTC can be calculated using the closed-form design equations in [50], which are rearranged into simpler forms as follows:

\[
C_s = \frac{2}{\omega_a \omega_b \left( \frac{Z_n \omega_a \tan \theta_a \sin \theta_a}{\tan \theta_a - \sin \theta_a} - \frac{Z_n \omega_b \tan \theta_b \sin \theta_b}{\tan \theta_b - \sin \theta_b} \right)}
\]

\[
C_p = \frac{1}{2\left( \omega_b^2 - \omega_a^2 \right)} \left( \frac{Y_n \omega_a \tan \theta_a \sin \theta_a}{\tan \theta_a - \sin \theta_a} - \frac{Y_n \omega_b \tan \theta_b \sin \theta_b}{\tan \theta_b - \sin \theta_b} \right)
\]

\[
L_s = \frac{1}{2\omega_a \omega_b \left( Y_n \omega_a \cot \frac{\theta_a}{2} - Y_n \omega_b \cot \frac{\theta_b}{2} \right)}
\]

\[
L_m = \frac{1}{2\omega_a \omega_b \left( Y_n \omega_a \cot \frac{\theta_a}{2} - Y_n \omega_b \cot \frac{\theta_b}{2} \right)}
\]

where \( Z_n \) and \( \theta_n \) are the characteristic impedance and electrical length of Line A at \( f_a \) while \( \theta_n \) are those of Line B at \( f_b \).

Based on (5)–(8), the required L and C values of six different BTC designs that are equivalent to two different transmission lines at \( f_a = 2.45 \) GHz and \( f_b = 5.8 \) GHz are shown in Table I (i.e., BTC\(_1\)–BTC\(_6\)). The results for a conventional wideband BTC design that is equivalent to a 50-\( \Omega \), 90\(^\circ\) line at 2.45 GHz are also included for comparison, in which \( f_a = 2.2 \) GHz and \( f_b = 2.7 \) GHz are used in solving the required L and C values to achieve a good match to a 50-\( \Omega \), 90\(^\circ\) line around 2.45 GHz with a proper bandwidth. For the conventional BTC design, the required mutual inductance \( L_m \) is positive, as shown in Table I. This is why the layouts
TABLE I

<table>
<thead>
<tr>
<th>Equivalent Transmission Line Impedance and Length</th>
<th>$L_m$(nH)</th>
<th>$L_s$(nH)</th>
<th>$C_T$(pF)</th>
<th>$C_p$(pF)</th>
<th>Realizable</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional Wideband Design of Bridged-T Coil</td>
<td>50 Ω, 90° at $f_c$ &amp; 50 Ω, 270° at $f_b$</td>
<td>1.79</td>
<td>0.59</td>
<td>1.90</td>
<td>0.24</td>
</tr>
<tr>
<td>BTC1</td>
<td>35.35 Ω, 90° at $f_c$ &amp; 35.35 Ω, 270° at $f_b$</td>
<td>1.47</td>
<td>-0.10</td>
<td>2.19</td>
<td>0.63</td>
</tr>
<tr>
<td>BTC2</td>
<td>50 Ω, 60° at $f_c$ &amp; 50 Ω, 170° at $f_b$</td>
<td>1.33</td>
<td>0.24</td>
<td>1.26</td>
<td>0.22</td>
</tr>
<tr>
<td>BTC3</td>
<td>50 Ω, 90° at $f_c$ &amp; 50 Ω, 170° at $f_b$</td>
<td>1.78</td>
<td>-0.11</td>
<td>1.64</td>
<td>0.61</td>
</tr>
<tr>
<td>BTC4</td>
<td>50 Ω, 90° at $f_c$ &amp; 50 Ω, 400° at $f_b$</td>
<td>1.83</td>
<td>2.79</td>
<td>3.70</td>
<td>-0.19</td>
</tr>
<tr>
<td>BTC5</td>
<td>50 Ω, 90° at $f_c$ &amp; 50 Ω, 400° at $f_b$</td>
<td>-10.25</td>
<td>-6.37</td>
<td>-1.33</td>
<td>-7.77</td>
</tr>
</tbody>
</table>

Table I

of conventional BTC designs in [46]–[53] are realized with a balanced spiral inductor. On the other hand, for BTC1 to BTC6, the value of $L_m$ can be either positive or negative, depending on the given specifications. In addition, under some extreme cases, e.g., BTC5 in Table I in which the magnitude of $L_m$ becomes larger than $L_s$, or BTC6 that requires negative $L_s$, $C_s$, and $C_p$, the resulted BTCs are not realizable in practice. Therefore, there are some design limits for the proposed dual-band design of BTC, which will be addressed in Section III. Still, there exists a wide range of realizable specifications as demonstrated in Table I as well as the design examples that will be given in Sections III and IV.

To examine the achievable performance of the proposed dual-band design of BTC, the circuit simulated response of BTC1 in Table I that is equivalent to a 50-Ω, 90° transmission line at 2.45 GHz and a 50-Ω, 270° transmission line at 5.8 GHz is shown in Fig. 2. The circuit simulated response of the conventional BTC design in Table I is also shown in Fig. 2, which is equivalent to a 50-Ω, 90° transmission line at 2.45 GHz. The simulated insertion losses of BTC1 at 2.45 and 5.8 GHz are both equal to 0 dB while the simulated insertion phases are equal to $-90°$ and $90°$ (or $-270°$) at these two frequencies, respectively. On the other hand, the conventional BTC features a much linear frequency response. Its simulated insertion loss is 0 dB at 2.45 GHz while the simulated insertion phase is $90°$. Although the simulated insertion loss of the conventional BTC is also 0 dB at 5.8 GHz, the simulated insertion phase becomes 164.8° or −195.2°. This is because the conventional BTC features an approximately linear frequency response, which can be told from the group delay response in Fig. 2(c). From the comparison of the two designs in Fig. 2, it is validated that the proposed dual-band design of BTC can indeed achieve the required line impedance and line length at the two selected frequencies.

As in the case of a conventional BTC, BTC1 can be conveniently realized using the integrated passive device (IPD) technology to achieve a very compact circuit size. Fig. 3 shows the simplified layer structure of the silicon-based IPD process employed in this paper, which is the same as that in [53]. This is a high-performance passive only process for RF and microwave applications. A high-resistivity silicon wafer is utilized as the substrate. The top metal (i.e., $M_3$) is 10-$\mu$m thick electroplated Cu, which can be used to realize high-performance spiral inductors and low-loss interconnections. The bottom metal layer $M_1$ of 1-$\mu$m thick is used for interconnection, under pass, and metal–insulator–metal (MIM) capacitor implementation along with the middle metal layer $M_2$. The NiCr layer is used to implement thin-film resistors. Such an IPD process is thus ideal for realizing high precision and high-quality RF embedded passive circuits.

The proposed BTC1 in Table I is first implemented by this IPD process to validate the actual performance. The proposed layout is shown in Fig. 4(a). Here, two spiral inductors on $M_3$ form the two series inductors $L_s$ in the circuit model
shown in Fig. 1(b). Since the required mutual inductance $L_m$ between them is negative (i.e., $L_m = -0.25 \text{nH}$), the layout of BTC1 is much different from those of the conventional BTCs in [46]–[53]. Specifically, the orientations of the two spiral inductors should be different such that a negative mutual inductance between them can be achieved. Therefore, they are placed side by side in the circuit layout with a proper spacing and a ground trace between them such that the required mutual inductance $L_m$ can be realized. Regarding the capacitors $C_s$ and $C_p$, they are conveniently realized using MIM capacitors formed between $M_1$ and $M_2$ in the IPD process.

The geometrical parameters of the layout in Fig. 4(a) are designed according to the following procedure. According to the required $L_s$, $C_s$, and $C_p$, the initial layout of two spiral inductors and MIM capacitors are first constructed with the aid of a quasi-static EM solver, e.g., Ansys Q3D. Since a small negative mutual inductance is required, the two spiral inductors are placed side by side with opposite orientation between them. A ground trace between the two spiral inductors can also be employed to reduce the mutual inductance if required. The MIM capacitors are then connected to their corresponding locations according to the circuit model of BTC in Fig. 1(b) to form the initial layout. Next, the electrical performance of the initial layout is simulated using a full-wave simulator, e.g., Ansys HFSS. The full-wave simulated $Z$- and $Y$-parameters at $f_a$ and $f_b$ are used to extract the equivalent $L$ and $C$ values of the initial layout using (1)–(4). The geometrical parameters of the spiral inductor and MIM capacitors are then adjusted until the extracted $L$ and $C$ values match with the design targets with minimum errors, and the layout design is thus completed.

The measured and EM simulated results of BTC1 are shown in Fig. 4(b)–(d) along with the IPD chip photograph. According to Fig. 4(b), it is quite matched to 50 $\Omega$ around the two desired frequency bands, and the measured return losses are 33.4 and 22.8 dB at 2.45 and 5.8 GHz, respectively. Low insertion loss is also obtained. The measured insertion loss is 0.57 dB at 2.45 GHz and it is 0.54 dB at 5.8 GHz. There is some discrepancy between the measured and EM simulation results, which is attributed to the fabrication error associated with the nitride thickness between $M_1$ and $M_2$. The measured and EM simulated insertion phase responses are shown in Fig. 4(c).

The measured insertion phase is $-93^\circ$ at 2.45 GHz and $87.2^\circ$ (or $-272.8^\circ$) at 5.8 GHz, which are quite close to the design targets.
The equivalent characteristic impedances of the BTC extracted using [55] are shown in Fig. 4(d). The equivalent characteristic impedance is $48 - j0.27 \Omega$ at 2.45 GHz and it is $53.4 - j1.31 \Omega$ at 5.8 GHz. According to the measured results, the proposed BTC design BTC1 in Fig. 4(a) can indeed achieve similar frequency characteristics as a 50-Ω, 90° transmission line at 2.45 GHz and a 50-Ω, 270° transmission line at 5.8 GHz except for some additional loss. Notably, the circuit size of BTC1 is only $1.282 \times 0.702$ mm, which is about $0.01\lambda_0 \times 0.0057\lambda_0$ at 2.45 GHz or $0.025\lambda_0 \times 0.014\lambda_0$ at 5.8 GHz. As will be shown in Sections III and IV, it can then be used to realize dual-band microwave passive components with very compact circuit sizes.

### III. Dual-Band Branch-Line Coupler

Based on the proposed dual-band design of BTC in Fig. 1(b), a miniature dual-band branch-line coupler design can be easily achieved. The circuit model of the proposed dual-band branch-line coupler is shown in Fig. 5(a), which is composed of two 50-Ω BTCs (BTC1) and two 35.35-Ω BTCs (BTC2). In addition, each of the BTCs is designed with a −90° insertion phase at $f_a$ and a −270° (or 90°) insertion phase at $f_b$ where $f_a < f_b$. The corresponding L and C values can then be found using (5) to (8). Here, $f_a = 2.45$ GHz and $f_b = 5.8$ GHz are chosen, and BTC1 and BTC2 in Table I are the required BTCs. The ideal frequency response of BTC1 has already been given in Fig. 2, while that of BTC2 is shown in Fig. 6. According to Fig. 6(a), BTC2 is well matched to 35.35 Ω at 2.45 and 5.8 GHz as expected. In addition, the insertion phase of BTC2 shown in Fig. 6(b) is equal to $-90°$ and $90°$ (or $-270°$) at 2.45 and 5.8 GHz, respectively. A dual-band branch-line coupler operated at 2.45 and 5.8 GHz can then be constructed using BTC1 and BTC2 according to the circuit topology shown in Fig. 5(a), and the corresponding circuit simulated frequency responses

---

**Fig. 5.** (a) Circuit model of the proposed miniature dual-band branch-line coupler based on BTCs. Circuit simulated frequency responses: (b) insertion loss, return loss, and isolation responses, (c) phase difference response for the low band, and (d) phase difference response for the high band.

**Fig. 6.** Circuit simulated responses of BTC2 in Table I. (a) Transmission and reflection coefficients. (b) Insertion phase and group delay. The reference impedances of the two-port S-parameters are equal to 35.35 Ω.
are shown in Fig. 5(b)–(d). A dual-band 3-dB hybrid coupler response is successfully obtained and the two passbands are correctly located at 2.45 and 5.8 GHz. In addition, the phase differences between the two outputs are both 90° at these two frequencies. For the low band, the input return loss, output return loss, and isolation are all better than 15 dB from 2.3 to 2.6 GHz, while the amplitude imbalance is better than 0.57 dB and the phase error is less than 5.1° in the same frequency range. For the high band, the input return loss, output return loss, and isolation are all better than 15 dB from 5.6 to 6 GHz, and the in-band amplitude imbalance is within 0.19 dB while the in-band phase error is less than 4°. Notably, the dual-band branch-line coupler in Fig. 5(a) is based on lumped element only, so its circuit size will be very small when implemented in IPD.

The realizable frequency ratio $f_b/f_a$ of the proposed dual-band branch-line coupler depends on the realizability of the...
BTCs. As shown in Table I, there are cases that the resulted \( L \) and/or \( C \) values are not achievable for the proposed dual-band design of BTC. Let \( f_a < f_b, 0° < \theta_a < \theta_b < 360°, \) and \( Z_a = Z_b \), the fundamental physical limitations of \( L_s \geq 0, |L_m/L_s| \leq 1, C_s \geq 0, \) and \( C_p \geq 0 \) lead to the following two design constraints:

\[
\frac{f_a \cot \theta_a}{2} \geq \frac{f_b \cot \theta_b}{2} \tag{9}
\]

\[
\frac{f_a \cot \theta_b}{2} \leq \frac{f_b \cot \theta_a}{2} \tag{10}
\]

For \( \theta_a = 90° \) at \( f_a \) and \( \theta_b = 270° \) at \( f_b \) used in the proposed dual-band branch-line coupler design, it appears that there is no limitation on the realizable frequency ratio \( f_b/f_a \). However, since a magnetic coupling coefficient with a magnitude \( M = |L_m/L_s| \) close to 1 is not achievable in practice, one should consider also the maximal realizable \( M \), i.e., \( M_{\text{max}} \) and set

\[
\left| \frac{L_m}{L_s} \right| \leq M_{\text{max}}. \tag{11}
\]

In this way, with \( Z_a = Z_b \), \( \theta_a = 90° \), and \( \theta_b = 270° \), the following lower and upper bounds of the frequency ratio \( f_b/f_a \) can be obtained using (7) and (8):

\[
\frac{f_b}{f_a} \geq \frac{3 + M_{\text{max}}}{1 + M_{\text{max}}} + \sqrt{\left( \frac{3 + M_{\text{max}}}{1 + M_{\text{max}}} \right)^2 - 4} \tag{12}
\]

\[
\frac{f_b}{f_a} \leq \frac{3 - M_{\text{max}}}{1 - M_{\text{max}}} + \sqrt{\left( \frac{3 - M_{\text{max}}}{1 - M_{\text{max}}} \right)^2 - 4}. \tag{13}
\]

As an example, for \( M_{\text{max}} = 0.7, 1.517 \leq f_b/f_a \leq 7.534 \) can be obtained, which becomes the realizable frequency ratio of the proposed dual-band branch-line coupler in Fig. 5(a).

The above design constraints can be verified using numerical examples. The calculated \( L \) and \( C \) values along with the magnetic coupling coefficient \( L_m/L_s \) of various BTC designs for \( \theta_a = 90°, \theta_b = 270°, Z_a = Z_b, \) and \( f_a = 2.45 \) GHz are shown in Fig. 7. It is clear that the \( L_s, C_s, \) and \( C_p \) are all larger than 0 while \( |L_m/L_s| < 1 \) as long as \( f_b/f_a > 1 \). On the other hand, if \( M_{\text{max}} = 0.7 \) is given, the realizable frequency ratio \( f_b/f_a \) will be limited within 1.517 and 7.534 as predicted by (12) and (13). Notably, according to Fig. 7(b), the range of realizable frequency ratio increases as \( M_{\text{max}} \) increases.

The proposed dual-band branch-line coupler with \( f_a = 2.45 \) GHz and \( f_b = 5.8 \) GHz in Fig. 5 is realized using the same IPD process shown in Fig. 3. For BTC\(_1\), the proposed BTC design in Fig. 4(a) is adopted. For BTC\(_2\), according to the required \( L \) and \( C \) values given in Table I, its circuit layout...
can be constructed in a similar way, and the result is shown in Fig. 8(a). A test circuit for BTC 2 is first realized in IPD, and the corresponding measured and EM simulated results are shown in Fig. 8(b)–(d). Here, the reference impedances of the two-port S-parameters are set as 35.35/Ω. According to the reflection coefficient responses in Fig. 8(b), BTC 2 is quite matched to 35.35/Ω around 2.45 and 5.8 GHz, and the measured return losses are 30.6 and 25.2 dB at these two frequencies, respectively. In addition, the measured insertion loss is 0.93 dB at 2.45 GHz and it is 0.97 dB at 5.8 GHz. The measured insertion phase in Fig. 8(c) is −92.1° at 2.45 GHz and 85.1° (or −274.9°) at 5.8 GHz.

The equivalent characteristic impedance of BTC 2 is shown in Fig. 8(d). It is equal to 35.8 − j0.39 Ω at 2.45 GHz and 35.5 − j0.42 Ω at 5.8 GHz, which is quite close to the design target of 35.35 Ω. The IPD-based dual-band BTC in Fig. 8(a) can thus achieve similar frequency characteristics as a 35.35-Ω, 90° transmission line at 2.45 GHz and a 35.35-Ω, 270° transmission line at 5.8 GHz except for the additional loss. In addition, a very compact circuit size is again achieved and BTC 2 is only 1.382 mm × 0.761 mm in size.

The two IPD-based BTC designs BTC 1 and BTC 2 in Figs. 4(a) and 8(a), respectively, are then combined to form the proposed miniature dual-band branch-line coupler in Fig. 9(a), and the chip photograph is shown in Fig. 9(b). Two of the ports (i.e., Ports 2 and 4) are properly oriented to allow the measurement of this dual-band branch-line coupler using a four-port vector network analyzer through on-wafer probing. The measured and EM simulated results are shown in Fig. 10, and the desired dual-band frequency characteristic is obtained as expected. The measured |S21| and |S31| are equal to −3.71 and −4.14 dB at 2.45 GHz, respectively, and they are equal to −3.36 and −4.61 dB at 5.8 GHz, respectively. The measured input and output return losses are all better than 15 dB from 2.25 to 2.55 GHz and from 5.55 to 5.95 GHz.
In addition, the measured isolation is better than 16.2 dB in the same frequency ranges.

The measured and EM simulated amplitude imbalance and phase difference responses are shown in Fig. 11. For the low band, the measured amplitude imbalance is within 0.43 dB from 2.25 to 2.55 GHz, and the measured phase error is within 3.9° in the same frequency range. As for the high band, the measured amplitude imbalance is within 1.25 dB and the measured phase error is within 5° from 5.55 to 5.95 GHz. The slightly larger amplitude and phase errors for the high band are mainly due to the fabrication error of the nitride layer. Table II shows a performance comparison of proposed dual-band branch-line coupler with other related recent works. Although the proposed design exhibits a moderate bandwidth and a slightly larger insertion loss due to the thinner conductor trace used in the IPD process, the proposed dual-band branch-line coupler features a much smaller circuit size of only 2.784 mm × 1.382 mm. Notably, the corresponding electrical size at \( f_1 = 2.45 \text{ GHz} \) (i.e., center frequency of the first passband) is only \( 0.0227\lambda_0 \times 0.0113\lambda_0 \) while that at \( f_2 = 5.8 \text{ GHz} \) is \( 0.0538\lambda_0 \times 0.0267\lambda_0 \). To the best of our knowledge, this is the smallest dual-band branch-line coupler ever reported.

### IV. Dual-Band Power Divider

The proposed dual-band design of BTC illustrated in Fig. 1(b) can also be applied to the realization of other miniature dual-band microwave passive components. As an
example, Fig. 12(a) shows the circuit model of proposed
miniature dual-band power divider. Here, two identical BTCs
with an equivalent characteristic impedance of 70.71 Ω
are employed, while the equivalent electrical length of the
BTC is designed as 90° and 270° at $f_a = 2.4$ GHz and
$f_b = 5.5$ GHz, respectively. In this way, the circuit model
in Fig. 12(a) can be equivalent to a conventional Wilkinson
power divider at both 2.4 and 5.5 GHz. A miniature dual-band
power divider based on lumped elements only can thus be
obtained.

Based on the above specifications, the required $L$ and $C$
values of the BTC can be obtained with the aid of (5) to (8),
and the results are:

- $L_s = 3.12$ nH
- $L_m = -0.57$ nH
- $C_s = 1.02$ pF
- $C_p = 0.37$ pF

The corresponding circuit simulation result is shown in Fig. 12(b). A power divider with
two passbands at 2.4 and 5.5 GHz is successfully achieved.

### TABLE II

<table>
<thead>
<tr>
<th>Process</th>
<th>[1]</th>
<th>[9]</th>
<th>[8]</th>
<th>[10]</th>
<th>[12]</th>
<th>[15]</th>
<th>[18]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB+SMD Component</td>
<td>PCB</td>
<td>PCB</td>
<td>PCB</td>
<td>PCB</td>
<td>PCB</td>
<td>PCB</td>
<td>Silicon-based IPD</td>
<td></td>
</tr>
<tr>
<td>$f_1/f_2$ (GHz)</td>
<td>0.92 / 1.74</td>
<td>2.45 / 5.25</td>
<td>2.36 / 5.7</td>
<td>1 / 2</td>
<td>2 / 4</td>
<td>3 / 5</td>
<td>0.87 / 1.79</td>
<td>2.45 / 5.8</td>
</tr>
<tr>
<td>Insertion Loss at $f_1$ (dB)</td>
<td>21.2 / 17.9</td>
<td>*25 / 18</td>
<td>*20 / 23</td>
<td>36.7 / 25.3</td>
<td>*25 / 20</td>
<td>16 / 16.4</td>
<td>26 / 21.6</td>
<td>21.6 / 18.5</td>
</tr>
<tr>
<td>for Through Port (dB)</td>
<td>3.7 / 4.0</td>
<td>3.3 / 3.4</td>
<td>3.9 / 4.4</td>
<td>3.3 / 3.1</td>
<td>3.9 / 4.6</td>
<td>3.4 / 4.2</td>
<td>3.3 / 3.67</td>
<td>3.7 / 3.4</td>
</tr>
<tr>
<td>Insertion Loss at $f_1$ for Coupled Port (dB)</td>
<td>3.6 / 3.6</td>
<td>3.4 / 4.1</td>
<td>3.1 / 3.7</td>
<td>4.1 / 4.0</td>
<td>3.09 / 3.9</td>
<td>4.1 / 4.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Isolation at $f_1/f_2$ (dB)</td>
<td>17.6 / 13.8</td>
<td>28 / 17</td>
<td>*32 / 26</td>
<td>32.9 / 29.9</td>
<td>*23 / 20</td>
<td>N.A.</td>
<td>34 / 19.9</td>
<td>26.9 / 24.8</td>
</tr>
<tr>
<td>Phase Error at $f_1$</td>
<td>1.4° / 1.0°</td>
<td>0.6° / 1.8°</td>
<td>0° / 1°</td>
<td>0° / 1°</td>
<td>3.5° / 2.8°</td>
<td>1.1° / 6.7°</td>
<td>0.7° / 1.4°</td>
<td>2.1° / 2.8°</td>
</tr>
<tr>
<td>Low-/High-Band 15-dB Return Loss Bandwidth</td>
<td>*6.7% / 4.5%</td>
<td>*43.2% / 12.5%</td>
<td>*9% / 4%</td>
<td>*14.3% / 7.2%</td>
<td>*21.3% / 8%</td>
<td>*4.9% / 7.8%</td>
<td>8.8% / 10.6%</td>
<td>12.5% / 6.96%</td>
</tr>
<tr>
<td>Circuit Area (mm$^2$)</td>
<td>~60 × 60</td>
<td>20 × 20</td>
<td>~65 × 61</td>
<td>~99.2 × 46.5</td>
<td>~26 × 7</td>
<td>~37 × 28</td>
<td>31 × 31</td>
<td>2.784 × 1.382</td>
</tr>
<tr>
<td>Electrical Size at $f_1$</td>
<td>0.184 × 0.184</td>
<td>0.163 × 0.163</td>
<td>0.511 × 0.479</td>
<td>0.330 × 0.155</td>
<td>0.173 × 0.047</td>
<td>0.370 × 0.280</td>
<td>0.090 × 0.090</td>
<td>0.0227 × 0.0113</td>
</tr>
<tr>
<td>Electrical Size at $f_2$</td>
<td>0.348 × 0.348</td>
<td>0.357 × 0.357</td>
<td>1.235 × 1.159</td>
<td>0.661 × 0.310</td>
<td>0.347 × 0.093</td>
<td>0.617 × 0.467</td>
<td>0.185 × 0.185</td>
<td>0.0538 × 0.0267</td>
</tr>
</tbody>
</table>

*Estimated from graph

### TABLE III

<table>
<thead>
<tr>
<th>Process</th>
<th>[25]</th>
<th>[34]</th>
<th>[36]</th>
<th>[29]</th>
<th>[30]</th>
<th>[32]</th>
<th>[41]</th>
<th>[45]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB + Chip Resistor</td>
<td>PCB + Chip Resistor</td>
<td>PCB + Chip Resistor</td>
<td>PCB + SMD Component</td>
<td>PCB + SMD Component</td>
<td>PCB + Chip Resistor</td>
<td>PCB + Chip Resistor</td>
<td>GaN</td>
<td>Silicon-based IPD</td>
<td></td>
</tr>
<tr>
<td>$f_1/f_2$ (GHz)</td>
<td>0.95 / 1.91</td>
<td>1 / 2</td>
<td>1.1 / 2.2</td>
<td>0.74 / 1.42</td>
<td>1 / 1.8</td>
<td>2.45 / 5.36</td>
<td>2.4 / 3.5</td>
<td>7 / 15</td>
<td>2.4 / 5.5</td>
</tr>
<tr>
<td>Insertion Loss at $f_1/f_2$ (dB)</td>
<td>&gt; 24 / 24</td>
<td>19.7 / 33.1</td>
<td>&gt; 25 / 25</td>
<td>31.8 / 44.6</td>
<td>&gt; 20 / 20</td>
<td>39.06 / 25.08</td>
<td>&gt; 20 / 20</td>
<td>N.A.</td>
<td>26.8 / 26.1</td>
</tr>
<tr>
<td>Output Return Loss at $f_1/f_2$ (dB)</td>
<td>&gt; 24 / 24</td>
<td>27.4 / 27.0</td>
<td>&gt; 25 / 25</td>
<td>23.1 / 34.8</td>
<td>&gt; 20 / 20</td>
<td>26.33 / 24.55</td>
<td>&gt; 18 / 20</td>
<td>N.A.</td>
<td>17.2 / 16.1</td>
</tr>
<tr>
<td>Insertion Loss at $f_1/f_2$ (dB)</td>
<td>*3.2 / 3.3</td>
<td>3.17 / 3.13</td>
<td>3.15 / 3.19</td>
<td>3.23 / 3.54</td>
<td>*3.10 / 3.18</td>
<td>3.20 / 3.53</td>
<td>3.94 / 3.77</td>
<td>N.A.</td>
<td>3.81 / 3.81</td>
</tr>
<tr>
<td>Isolation at $f_1$</td>
<td>&gt; 28 / 28</td>
<td>26.4 / 30.5</td>
<td>&gt; 30 / 30</td>
<td>41.8 / 27.8</td>
<td>&gt; 20 / 20</td>
<td>39.73 / 33.53</td>
<td>&gt; 20 / 20</td>
<td>N.A.</td>
<td>22.9 / 23.6</td>
</tr>
<tr>
<td>Low-/High-Band Return Loss (RL &gt; 15 dB) Bandwidth</td>
<td>6.3% / 3.1% (RL &gt; 15 dB)</td>
<td>*25% / 24% (RL &gt; 20 dB)</td>
<td>*41% / 19% (RL &gt; 20 dB)</td>
<td>41.2% / 20.7% (RL &gt; 15 dB)</td>
<td>*40% / 25.7% (RL &gt; 20 dB)</td>
<td>*19% / 5.8% (RL &gt; 15 dB)</td>
<td>*5.3% / 8.2% (RL &gt; 15 dB)</td>
<td>N.A.</td>
<td>53.6% / 17.7% (RL &gt; 15 dB)</td>
</tr>
<tr>
<td>Circuit Area (mm$^2$)</td>
<td>~37 × 37</td>
<td>~23.6 × 48</td>
<td>4 × 59</td>
<td>21 × 119</td>
<td>~25 × 114</td>
<td>~20 × 20</td>
<td>~20 × 28</td>
<td>~0.68 × 0.54</td>
<td>1.814 × 1.666</td>
</tr>
<tr>
<td>Electrical Circuit Area at $f_1$ ($\lambda_0^2$)</td>
<td>0.117 × 0.117</td>
<td>0.079 × 0.16</td>
<td>0.014 × 0.216</td>
<td>0.052 × 0.294</td>
<td>0.083 × 0.38</td>
<td>0.163 × 0.163</td>
<td>0.160 × 0.224</td>
<td>~0.0158 × 0.0126</td>
<td>0.0145 × 0.0133</td>
</tr>
<tr>
<td>Electrical Circuit Area at $f_2$ ($\lambda_0^2$)</td>
<td>0.236 × 0.236</td>
<td>0.157 × 0.32</td>
<td>0.029 × 0.433</td>
<td>0.099 × 0.563</td>
<td>0.15 × 0.68</td>
<td>0.357 × 0.357</td>
<td>0.233 × 0.327</td>
<td>~0.034 × 0.027</td>
<td>0.0333 × 0.0305</td>
</tr>
</tbody>
</table>

*Estimated from graph
For the low band, the simulated input return loss, output return loss, and isolation are all better than 20 dB from 2.2 to 2.7 GHz, while the corresponding simulated in-band insertion loss is better than 3.05 dB. As for the high band, the simulated input return loss, output return loss, and isolation are better than 20 dB from 5 to 6.2 GHz, and the simulated in-band insertion loss is better than 3.05 dB.

Fig. 13(a) shows the layout of the 70.71-Ω BTC for use in the proposed dual-band power divider design, which is also implemented in the same IPD process. The corresponding measured and EM simulated results are shown in Fig. 13(b)–(d). Again, it can achieve a good match to the desired line impedance and line length at 2.4 and 5.5 GHz. The proposed dual-band power divider can then be realized by employing the BTC design in Fig. 13(a) along with a thin-film isolation resistor $R = 100$ Ω, and the IPD chip layout is shown in Fig. 14(a). Here, the orientations of Ports 2 and 3 are properly arranged to facilitate the measurement of the dual-band power divider using on-wafer probing.

The measured and EM simulated results are shown in Fig. 15, and the desired dual-band power divider frequency characteristic has been obtained successfully. The agreements between the measured and EM simulated output return losses as well as the isolation responses are not good, which are mainly due to the fabrication error of the isolation resistor. As shown in Fig. 16, much better matches between the measured and EM simulated output return loss and isolation can be obtained by increasing the isolation resistor in the EM simulation to $R = 160$ Ω instead of the originally designed value of 100 Ω. Despite that the measured output return loss and isolation are not as good as the EM simulated ones, the measured input return loss, output return loss, and isolation of the proposed dual-band power divider are all better than 15 dB from 1.85 to 3 GHz for the low band and from 5 to 5.8 GHz for the high band. In addition, the measured insertion loss is better than 3.94 dB within these two frequency bands. Notably, the circuit size of this dual-band power divider is only 1.814 mm × 1.666 mm, which is about 0.0145λ0 × 0.0133λ0 at $f_1 = 2.4$ GHz and 0.0333λ0 × 0.0305λ0 at $f_2 = 5.5$ GHz.

Table III shows the performance comparison of the proposed dual-band power divider with other related recent works. The proposed dual-band power divider features a much smaller circuit size compared to all other designs in Table III except [45].
On the other hand, its electrical circuit size is about the same as the lumped-element-based design using the GaN technology in [45], which is the current state of the art for the miniature dual-band power divider design. As for the realizable frequency ratio $f_b/f_a$ of proposed dual-band power divider design, it is also limited by the realizability of the BTCs, which can be examined using (12) and (13) in Section III.

In our previous works on miniature microwave circuit designs based on BTCs, e.g., [46]–[53], BTCs are used to replace transmission line sections in microwave circuit designs such that almost identical frequency characteristic can be achieved while reducing the circuit size. On the other hand, with the proposed dual-band design method of BTC, a single-band circuit can be turned into a dual-band one by replacing the transmission line sections with BTCs. Especially, all the proposed design equations are closed-form ones. This much simplifies the realization of dual-band microwave circuits. In addition, the resulted dual-band circuit will be based on lumped elements only, which can be implemented in a very compact circuit size as demonstrated in this paper.

V. CONCLUSION

In this paper, a simple synthesis method to achieve the dual-band design of BTC has been proposed. BTCs with the desired insertion phase and line impedance at two different frequencies have been successfully demonstrated. Miniature dual-band microwave passive components can then be easily achieved by employing the proposed dual-band design of BTC to replace the transmission line sections in the original single-band circuit. Specifically, miniature dual-band branch-line coupler and dual-band power divider in IPD technology have been successfully demonstrated. The proposed design method can also be extended to the size reduction of other dual-band microwave circuits to largely reduce their circuit sizes.

REFERENCES


Wei-Ting Fang (S’16) was born in Taipei, Taiwan, in 1984. He received the B.S. degree in electrical engineering from National Chiao Tung University, Chia Yi, Taiwan, in 2011, and the Ph.D. degree from the Department of Electrical Engineering, National Central University, Taoyuan, Taiwan, in 2017. His current research interests include the design of compact microwave circuits and RF system-in-package modules.

En-Wei Chang was born in Taipei, Taiwan, in 1993. He received the B.S. degree in electrical engineering from National Chung Cheng University, Chia Yi, Taiwan, in 2015. He is currently pursuing the M.S. degree at the Department of Electrical Engineering, National Central University, Taoyuan, Taiwan. His current research interests include the designs of compact RF passive components and microwave circuits.

Yo-Shen Lin (M’04–SM’08) was born in Taipei, Taiwan, in 1973. He received the B.S. and M.S. degrees in electrical engineering and Ph.D. degree in communication engineering from National Taiwan University, Taipei, in 1996, 1998, and 2003, respectively. From 1998 to 2001, he was an RF Engineer with Acer Communication and Multimedia Inc., Taipei, where he was involved in designing global system for mobile communication (GSM) mobile phones. From 2001 to 2003, he was with Chi-Mei Communication System Inc., Taipei, where he was involved in the design of low-temperature co-fired ceramic RF transceiver modules for GSM mobile applications. In 2003, he joined the Graduate Institute of Communication Engineering, National Taiwan University, as a Post-Doctoral Research Fellow, and became an Assistant Professor in 2004. Since 2005, he has been with the Department of Electrical Engineering, National Central University, Taoyuan, Taiwan, where he is currently a Professor and the Associated Chair of the department. From 2010 to 2013, he was the Director of the Top University Program Office under the Research and Development Office, National Central University. In 2008, he joined the Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik, Berlin, Germany, as a Guest Researcher, and in 2014, he joined the Department of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA, USA, as a Visiting Scholar. He has authored or co-authored over 120 international journal and conference papers and holds 5 granted U.S. patents. His current research interests include the designs of miniature microwave passive components and highly integrated RF transceiver modules for wireless communication applications.

Prof. Lin was a recipient of the Best Paper Award of the 2001 Asia-Pacific Microwave Conference, Taipei, the URSI Young Scientist Award presented at the 2005 URSI General Assembly, New Delhi, India, the URSI EMT-S Young Scientist Award presented at the 2007 URSI International Electromagnetic Symposium (EMT-S), Ottawa, ON, Canada, the 2008 Exploration Research Award of the Pan Wen-Yuan Foundation, Taiwan, the 2012 Outstanding Young Electrical Engineer Award of the Chinese Institute of Electrical Engineering, Taiwan, and the Best Symposium Paper Award of the 2015 Asia-Pacific International Symposium on Electromagnetic Compatibility, Taipei. Since 2017, he has been the Vice Chair of the Taipei Chapter of the IEEE MTT-S.
学霸图书馆（www.xuebalib.com）是一个“整合众多图书馆数据库资源，
提供一站式文献检索和下载服务”的24小时在线不限IP图书馆。
图书馆致力于便利、促进学习与科研，提供最强文献下载服务。

图书馆导航：
图书馆首页 文献云下载 图书馆入口 外文数据库大全 疑难文献辅助工具