Punch-through impact ionization MOSFET (PIMOS): From device principle to applications

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**Abstract**

In the present work a punch-through impact ionization MOSFET (PIMOS) is presented, which exploits impact ionization in low-doped body-tied Ω- and tri-gate structures to obtain abrupt switching (3–10 mV/decade) combined with a hysteresis in the \( I_d(V_{DS}) \) and \( I_d(V_{GS}) \) characteristics. The PIMOS device shows an extraordinary temperature stability up to 125 °C. The influence of various parameters on device performance as abrupt switch or memory cell is investigated. Reduction of the electrical channel length, i.e. of gate length and/or substrate doping, reduces the breakdown voltage and hence the DRAM operating performance as abrupt switch or memory cell is investigated. Reduction of the electrical channel length, i.e. of gate length and/or substrate doping, reduces the breakdown voltage and hence the DRAM operating voltage, but also increase the \( I_{LS} \). Two architectures for a capacitor-less DRAM cell are demonstrated and evaluated. In addition, a PIMOS n-type hysteretic inverter is demonstrated, which may serve as a 1T SRAM cell.

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1. Introduction

The subthreshold slope of a MOSFET determines the ability to turn on and off the device. At room temperature the ideal value is 60 mV/decade, which is determined by diffusion of carriers from the source to the channel [1]. However, with continued scaling and corresponding reduction of bias voltages, the subthreshold slope found in actual devices is generally greater than this ideal value. In order to overcome this limitation there has been a great interest in alternative devices based on fundamentally different operation mechanisms that result in a transition between the off and on state of an electronic switch, which is more abrupt than 60 mV/decade at room temperature. The IMOS, first presented in [2] relies on an amplification of the on level by avalanche multiplication, to reduce the slope, whereas in the tunnel-FET [3] the leakage current is reduced by using tunneling as the transport mechanism.

Recently, we proposed the punch-through impact ionization MOSFET (PIMOS) in [4] which, like the IMOS, relies on avalanching to obtain slopes of 3–10 mV/decade, but which in addition presents a hysteresis behavior in both the \( I_d(V_{DS}) \) and \( I_d(V_{GS}) \) characteristics.

The IMOS presented in [2,5] is basically a gated p-i-n structure, where the gate voltage is used to adjust the diode breakdown voltage. The main advantage is the ability to amplify \( I_{on} \) while keeping \( I_{sat} \) low, however reliability is an issue due to the proximity of the avalanche generated carriers and the gate oxide, though this can be improved by a vertical structure [6]. The fact that the \( V(I) \) characteristic do not saturate, results in an inverter performance which is not superior to that of CMOS [5,7]. The PIMOS structure, is identical to that of a MOSFET, even though the optimization of device parameters differs from good scaling rules of conventional CMOS [8]. Thus in order to obtain the hysteresis characteristic following impact ionization, the device must be biased in punch-through and enable a parasitic bipolar latch, i.e., either low doping and/or short channel lengths are required.

In the present work, we will discuss the functionality of the PIMOS in greater detail based on: (i) TCAD simulations that are used to investigate the influence of various parameters on device performance and the ultimate scalability of the device, and (ii) experimental results corresponding to Ω-gate, tri-gate and quasi-planar body-tied PIMOS transistors.

2. Device principle

The PIMOS device structure investigated in this work is represented in Fig. 1, it is designed as a conventional NMOS with a very low-doped body/channel region \( N_A < 10^{15} \text{ cm}^{-3} \) and fairly abrupt N+ region (arsenic doped, \( \sim 10^{20} \text{ cm}^{-3} \)). The body of the device is shaped as an Ω- or tri-gate for small widths, \( W \), and develops gradually into a quasi-planar device for large \( W \).

For low drain bias the PIMOS operates as a conventional MOSFET, as \( V_{DS} \) is increased impact ionization will take place at the drain-substrate junction and the drain current will increase rapidly; so far this could resemble the operation of a MOSFET at very high drain bias. However, if at the moment when avalanching sets in the condition of punch-through is met and the device is biased...
in subthreshold, $V_{GS} < V_T$, the particular PIMOS functionality will set in, because the electrostatic potential in the channel creates a saddle point in the channel near the drain junction as first reported in [9], see Fig. 2. The electrons generated by impact ionization are swept into the drain junction, whereas, the holes can be separated into two fractions.

Part of the holes will migrate towards the point of lowest potential creating a hole pocket at the interface, this also causes a displacement away from the interface of the electron current, see Fig. 3a in which the current distribution at breakdown differs from that of the conventional MOSFET in Fig. 3b. The filling of the hole pocket at the saddle point will result in an increase of the body potential, and hereby a decrease of the local threshold voltage as a function of the drain potential. A similar effect can be observed in partially depleted (PD) SOI devices, which results in very abrupt inverse subthreshold slope, when the threshold voltage is reduced.

Another part of the holes constitutes a substrate current, which causes a voltage drop across the substrate resistance, $R_{sub}$, that will eventually forward bias the source-substrate junction and turn on the parasitic bipolar structure. The bipolar gain will result in a further amplification of the base (substrate) current, and hence also the channel current. This constitutes a positive feedback loop on the current flowing through the device, leading to an abrupt increase of the drain current and thus a steep inverse subthreshold slope.

Hence at breakdown the total drain current is given by the sum of the MOSFET channel current, $I_{ch}$, and the parasitic bipolar collector current, $I_C$ multiplied by the avalanche multiplication factor, $M$ [14]. When operated in subthreshold $I_{th}$ is equal to the MOSFET subthreshold leakage current at the given $V_{DS}$, whereas in the inversion regime $I_{th} = I_{omega}$.

$$I_D = M(I_{ch} + I_C)$$

The hysteresis observed in a reverse scan of both the $I_D(V_{GS})$ and the $I_D(V_{DS})$ characteristics is due to a combination of the impact ionization under the high drain bias and the positive feedback loop sustained by the BJT action. When the positive feedback loop can no longer be maintained the drain current will drop suddenly. If the drain current is large enough the positive feedback loop cannot be turned off within a reasonable value of $V_{GS}$ and the current stays latched in the high level in the $I_D(V_{GS})$ characteristics. Latching is not possible in the $I_D(V_{DS})$ characteristics, as it is primarily the $V_{DS}$ bias which determines the impact ionization.
Fig. 4 shows a typical experimental hysteresis in $I_D(V_{DS})$ at high $V_{DS}$, where impact ionization dominates. By careful tuning of the $V_{GS}$ bias to be within the hysteresis loop, a hysteresis in the $I_D(V_{GS})$ can also be obtained, see Fig. 5.

When $V_{DS}$ is close to $V_{DBD}$ an increase in $V_{GS}$ will increase the drain current, and thereby also the amount of carriers available for impact ionization. This will result in sufficient current for the turn-on of the parasitic bipolar action. With increasing gate bias, however, the drain saturation voltage $V_{DS}^{sat}$ will significantly increase as well, hereby reducing the excess drain bias $V_{DS} - V_{DS}^{sat}$. This will reduce the maximum field near the drain and, hence, the impact ionization current [15]. The $I_D(V_{GS})$ hysteresis is much more sensitive to the actual value of $V_{DBD}$.

In the following, the notation drain breakdown voltage, $V_{DBD}$, is used when referring to the physical breakdown of the device at high $V_{DS}$ bias. Whereas, the pull-up and pull-down voltages in the $I_D(V_{DS})$ and $I_D(V_{GS})$, $V_{GPU}$, $V_{DPD}$, $V_{GPU}$, and $V_{GDPU}$ are used to describe the abrupt transition region in the hysteresis characteristics. Note that for the PIMOS $V_{DPDU} = V_{DBD}$.

3. Fabrication

The PIMOS devices are fabricated according to the process flow depicted in Fig. 6. This process-flow shows the development of an $\Omega$-cross-section, however, in addition also gate-all-around as well as tri-gate devices have been fabricated with a similar process, each presenting their own advantages. Gate-all-around MOSFETs show enhanced mobility due to oxidation induced strain [16], which is not present in body-tied structures. However, as a body contact is required for PIMOS operation this is only possible on $\Omega$- and tri-gate structures. Similar abrupt switching and hysteresis is observed in both the $\Omega$-tri-gate and quasi-planar devices designed with $W$ so large (up to 40 $\mu$m) that the influence from the side gates is negligible. Based on this observation it is concluded that the device principle is also valid for quasi-planar structures and TCAD simulations are carried out on 2D structures. Since, multi-gate structures are known to offer an improved control of short-channel effects, this is most likely also true for the punch-through impact ionization phenomenon. The hysteresis in $I_D(V_{GS})$ appears less critically dependent on the exact value of $V_{DS}$ and hence more controllable in more compact devices, but we have not established the exact correlation yet.

The substrate is lowly doped (high-resistivity: 15–25 $\Omega$ cm) p-type bulk silicon. A silicon rib of 0.3–1 $\mu$m depth is first dry-etched using fluorine chemistry and a hard mask of 15 nm SiO$_2$ and 80 nm Si$_3$N$_4$.

A sacrificial oxidation of 300 nm grown oxide is performed in order to smooth the sidewalls (to attenuate etching non-uniformity), and to reduce the horizontal dimensions in a controllable fashion. The sacrificial oxide is removed in a buffered HF (BHF) bath and 35 nm thick nitride spacers are deposited and etched. An isotropic silicon etch is used to partially underetch the nanowire, as illustrated in Fig. 6 step 3. The nitride hard mask is removed along with the oxide in a HF-bath. A second oxidation follows to repair any etching damage and reduce the dimensions even further. The thermal oxide is removed and replaced by a deposited LPCVD low temperature oxide (LTO). The LTO is

Fig. 4. Experimental abrupt switching and hysteresis in $I_D(V_{DS})$ characteristic for a device of $L = 1.4 \mu$m and width $W = 40 \mu$m, for $V_{GS} = 0.5 \text{ V}$ and $V_{DS} = 0 \text{ V}$. Inset shows a zoom of the hysteresis. The slopes $S_C$ and $S_S$ are defined as the inverse of the logarithmic low-high and high-low transients in $I_D(V_{DS})$ and $I_D(V_{GS})$, respectively, similarly to the subthreshold slope for a MOSFET.

Fig. 5. (a) Abrupt switching and hysteresis in $I_D(V_{DS})$ (solid line) and $I_D(V_{GS})$ (dotted line) measured in a 4.2 $\mu$m long and 2 $\mu$m wide device, $t_{ox} = 20 \text{ nm}$, $V_{GS} = 0.5 \text{ V}$. Device threshold voltage is $V_t \approx 0 \text{ V}$; (b) zoom on the hysteresis curve for $V_{DS} = 11.6 \text{ V}$ and $V_{DS} = 0 \text{ V}$; (c) Transconductance peaks extracted for the three curves in (a) showing the very sharp increase at the switching points.
planarized in a chemical–mechanical polishing (CMP) step, and partially removed to expose the silicon Ω-structure in the regions where the MOSFET is implemented. An oxide is maintained on the silicon bulk surface to isolate the device.

A gate stack consisting of 10–20 nm thermal oxide and 100–500 nm poly-silicon is created. The poly-silicon gate is patterned and isotropically etched, and a self-aligned arsenic implantation of gate, source and drain is carried out. The doping is activated by an annealing step at 950 °C for 10 min. For the devices with thin poly-layers (100 nm) a part of the gate on the lower concave part of the sidewalls is practically un-doped, as shown in Fig. 7, due to the 3D geometry of the device in combination with the low diffusivity of arsenic. This results in some high \( I_{\text{off}} \), which can be controlled by the substrate bias in longer devices [17].

4. Electrical characteristics

For low drain voltages the device operates as a conventional short-channel MOSFET, Fig. 8 shows \( I(V) \) characteristics for the MOSFET region of operation of a PIMOS device, \( I_{\text{on}} \) is on the order of 100 μA/μm at \( V_{\text{GS}} = V_{\text{DS}} = 2 \) V and the extracted low-field mobility is about 500 cm²/Vs. In the \( I_{\text{off}}(V_{\text{DS}}) \) MOSFET characteristics, Fig. 8b, the spacing of the different \( V_{\text{GS}} \) levels indicate some carrier velocity saturation in the intrinsic channel. Since short-channel effects are inherent to device operation, there will also be a fairly high leakage current, \( I_{\text{off}} \) at \( V_{\text{GS}} = V_{\text{DS}} = 1 \) V for the devices presented here, see Fig. 8a.

When the short-channel device is biased in subthreshold and a large \( V_{\text{DS}} \) bias is applied (\( \geq 8 \) V, depending on geometry for fabricated devices), impact ionization and avalanching will take place near the drain and the voltage drop across the substrate resistance \( R_{\text{sub}} \) will turn on the parasitic bipolar. This turn-on of the parasitic bipolar can be observed in the snapback characteristics in Fig. 9, where it gives rise to a negative resistance. The gain of the parasitic bipolar

![Fig. 6. Process flow showing a cross-section through the channel. (1) Anisotropic rib etching with hard mask. (2) Sacrificial oxidation. (3) Nitride spacer. (4) Oxidation. (5) LTO deposition. (6) CMP planarization and BHF oxide etch to liberate Ω-device. (7) Gate oxide growth (10 nm) and poly silicon deposition. (8) Poly-Si patterning and As implantation. The FIB images to the left shows cross-sections for different devices corresponding to processing steps 3, 4 and 7.](image1)

![Fig. 7. Finite element cross-section simulation, with arsenic doping in poly-silicon. Inset shows a FIB cross-section of fabricated Ω-gate device on which we modeled the simulation.](image2)

![Fig. 8. Characteristics for the MOSFET region of operation of a quasi-planar PIMOS, \( L = 1.4 \) μm, \( t_{\text{ox}} = 10 \) nm and width \( W = 40 \) μm. (a) \( I_{\text{d}}(V_{\text{GS}}) \) for various drain bias. (b) \( I_{\text{d}}(V_{\text{DS}}) \) characteristics.](image3)

![Fig. 9. Drain current snapback in \( V_{\text{GS}} \) (solid line) measured using current biasing. Dotted lines show the corresponding hysteresis in \( I_{\text{d}} \) and \( I_{\text{B}} \) measured using standard voltage biasing (\( V_{\text{GS}} = 0 \) V). Snapback demonstrates that the bipolar effect dictates the high-level transition of the hysteresis loop in PIMOS. \( L = 1.4 \) μm and \( W = 10 \) μm.](image4)
bipolar transistor has a value of around 10, which varies from one device to another according to their geometry.

By tuning of $V_{DS}$ to a value within the hysteresis profile, the hysteresis can also be reproduced in the $I_D(V_{GS})$ characteristic, see Fig. 5. The latch is an extreme case of the hysteresis in $I_D(V_{GS})$, Fig. 5a, when $V_{DS}$ is large enough that the pull-down is not reached within a reasonable $V_{GS}$ value, and $I_D$ stays high.

Fig. 10a shows the $I_D(V_{GS})$ hysteresis curves for increasing values of gate bias. As $V_{GS}$ is increased $V_{DBD}$ decreases and eventually the hysteresis disappears when we move into strong inversion. A slightly negative $V_{GS}$ can increase the hysteresis even further, but as we move into subthreshold this effect quickly diminishes and $V_{DBD}$ saturates. This corresponds well with simulations of the breakdown voltage as a function of gate bias for three different doping levels, shown in Fig. 10b for a 1 $\mu$m long device. In deep subthreshold the dependence of breakdown voltage on $V_{GS}$ is very small. When $V_{CS}$ approaches the threshold voltage this shifts to a decrease in $V_{DBD}$ with increasing $V_{CS}$ which continues well into moderate inversion.

5. High temperature operation

The PIMOS devices have been tested from room temperature up to 135 °C. In the following we present the investigation of temperature effect in a quasi-planar device with $L = 1.4 \mu m$ and $W = 40 \mu m$. For normal MOSFET operation the threshold voltage drops off with around $-0.9$ V/°C, and the subthreshold slope for this device increases from around 85 to 165 mV/dec. when the temperature is increased from 35 to 135 °C, altogether a decent MOSFET performance.

The PIMOS $I_D(V_{DS})$ high temperature characteristics are shown in Fig. 11. From room temperature and up to 115 °C the hysteresis remains very stable, the shift in breakdown voltage over the entire range is around 250 mV, but there is no clear trend neither decreasing nor increasing with temperature. When the device performance eventually deteriorates around 125 °C, this is due to a rapid increase in the gate current, so we estimate that the limit of high temperature performance in our case is caused by oxide breakdown rather than the intrinsic PIMOS performance. The substrate current increases monotonically with increasing temperature. In the drain current we observe a point of zero temperature change (ZTC) before the breakdown. This is due to the different temperature dependence of the subthreshold MOSFET current, $I_{DS}^{sub}$, which increases with increasing temperature; and the impact ionization current, which decreases with increasing temperature. The small shift in breakdown voltage $V_{DBD}$ corresponds well to TCAD simulations carried out for a comparable 2D geometry, shown in Fig. 12. For temperatures above room temperature ($T = 300$ K) the drain breakdown voltage increases with temperature as shown with a rate of approximately 4 mV/K. This dependence is also expected, as the temperature increases the free carriers will lose an increasing amount of energy to the lattice since the electron-phonon mean free path decreases. When the carrier energy available for impact ionization is reduced the impact ionization efficiency will decrease.

Fig. 10. (a) Effect of the gate bias on the $I_D(V_{CS})$ breakdown voltage and hysteresis, measured at $V_{BS} = 0$ V on a device with $L = 4.2 \mu m$ and $W = 2.5 \mu m$. $V_I \sim 0.2$ V. (b) Simulation of the breakdown voltage as a function of gate bias for three different doping levels, the vertical dashed lines indicate the threshold voltage.

Fig. 11. Effect of temperature (from 25° to 125°) on $I_D$ (solid lines) and $I_B$ (dotted lines) hysteresis for a PIMOS device with $L = 1.4 \mu m$ and $W = 40 \mu m$, $V_{GS} = -0.5$ V and $V_{BS} = 0$ V. Notice the point of zero temperature-change ZTC in the $I_D$ characteristics.

Fig. 12. Simulation of breakdown voltage as a function of substrate temperature for two different biasing conditions – both in subthreshold. $L = 1.5 \mu m$, $W = 1 \mu m$, $N_A = 10^{15}$ cm$^{-3}$ and $t_{ox} = 10$ nm.
6. Scalability

The scalability of PIMOS devices is discussed here from the point of view breakdown voltage reduction and channel length influence on the hole pocket control. The proposed analysis is aimed at device optimization.

As stated previously, short-channel effects are inherent to the PIMOS device, so the scalability is mainly limited by the \( l_{\text{tot}} \). As shown in Fig. 13 the breakdown voltage can be effectively reduced by reducing the channel length, but this results in deteriorated subthreshold slope in the MOSFET region of operation \((V_{\text{DS}} = 50 \text{ mV})\).

Fig. 14 shows the simulated drain breakdown voltage and the amount of short-channel effect expressed as \( \Delta L = L - L_{\text{min}} \), which is the difference in length between the actual device channel length, \( L \), and the minimum length before short channel effects sets in, \( L_{\text{min}} \), given by [18] as,

\[
L_{\text{min}} = 0.4|x|t_{\text{ox}}(W_{\text{S}} + W_{\text{D}})^{2}/t_{\text{ox}}^{1/3}
\]

where \( x \) is the junction depth, \( t_{\text{ox}} \) the gate oxide thickness and \( W_{\text{S}} \) and \( W_{\text{D}} \) are the depletion widths of the source and drain junction. When \( \Delta L \) is equal to zero the device should be at the onset of short-channel effects. However, one should note that this is only an empirical estimate. In any case, two regions of operation are clearly distinguished. For low doping, i.e., devices presenting short-channel effects, the breakdown voltage is reduced with decreasing doping density as the substrate resistance is increased so a smaller avalanche current is required to forward bias the source-substrate junction, in addition punch-through of the channel will also happen at a lower \( V_{\text{DS}} \).

Shown in Fig. 15 are the breakdown voltage and subthreshold leakage for four different doping profiles, including two graded profiles. In CMOS technologies retrograde wells, where the doping level increases towards the bulk, are used to reduce the risk of latch-up [19], and similar profiles are used for threshold voltage control in scaled MOSFETs [20]. The approach here is the contrary; the doping density is increased at the surface to reduce the MOSFET leakage, and the doping is reduced towards the substrate to increase the substrate resistance, thereby reducing the required substrate current to forward bias the source-substrate junction. A graded channel doping profile, easily obtainable by an implantation/diffusion step, can significantly improve the PIMOS properties compared to a constant channel doping. When considering Fig. 15, a simple doubling of the channel doping from \( 5 \times 10^{16} \text{ cm}^{-3} \) to \( 10^{17} \text{ cm}^{-3} \) might reduce the leakage current by 77%, but will also increase the breakdown voltage by 34%. By using a graded profile going from \( 2.5 \times 10^{17} \text{ cm}^{-3} \) at the surface to \( 5 \times 10^{16} \text{ cm}^{-3} \) at a depth of ~30 nm (case 3), the same reduction in leakage current (77%) can be obtained, but with a much smaller increase in \( V_{\text{BD}} \) of only 13%, and the subthreshold slope remains unchanged.

![Fig. 13](image-url) Simulated breakdown voltage and subthreshold slope as a function of gate length for a device of \( L = 1.5 \mu m, t_{\text{ox}} = 10 \text{ nm} \) and \( N_{A} = 10^{19} \text{ cm}^{-3} \), compared with experimentally extracted values of the breakdown voltage. The shifted values around \( L = 1.5 \mu m \) are due to a difference in oxide thickness.

![Fig. 14](image-url) Drain breakdown voltage and \( \Delta L \) as a function of substrate doping simulated on two devices of different length, but with same junction depth and oxide thickness, \( t_{\text{ox}} = 10 \text{ nm} \) and \( x_j = 170 \text{ nm} \).

![Fig. 15](image-url) (a) Four different doping profiles investigated, nominated case 1–4 (1) constant at \( 5 \times 10^{16} \text{ cm}^{-3} \) (2) graded from 1.5 \( \times 10^{17} \text{ cm}^{-3} \) at the surface to \( 5 \times 10^{16} \text{ cm}^{-3} \) in the bulk (3) graded from \( 2.5 \times 10^{17} \text{ cm}^{-3} \) at the surface to \( 5 \times 10^{16} \text{ cm}^{-3} \) in the bulk (4) constant at \( 10^{17} \text{ cm}^{-3} \), \( L = 300 \text{ nm} \), \( x_j = 80 \text{ nm} \) and \( t_{\text{ox}} = 2 \text{ nm} \). (b) Breakdown voltage and subthreshold leakage \((V_{\text{DS}} = 0 \text{ V} < V_{\text{t}} \), \( V_{\text{DS}} = 2 \text{ V} \)).
Based on the dependence on various parameters we have simulated a scaled PIMOS device, the cross-section of which can be seen in Fig. 16 at the point of breakdown. The dimensions for this scaled device are: \( L = 100 \text{ nm}, \ t_{ox} = 2 \text{ nm} \) and the channel incorporates a graded doping profile from \( 5 \times 10^{17} \text{ cm}^{-3} \) at the surface to \( 2 \times 10^{16} \text{ cm}^{-3} \) in the bulk. The breakdown voltage in this case is only 5.96 V, the current level at \( V_{in} = 2 \text{ V} \) (\( V_{CS} = 0 \text{ V} < V_T \)) is quite high at \( \approx 2.5 \mu A \), but further optimization should be possible. However the bulk breakdown mechanism is clearly visible in the figure.

Fig. 16. TCAD simulation of the electron current distribution in a very scaled device \( L = 100 \text{ nm}, \ t_{ox} = 2 \text{ nm} \) and the doping density in the channel is graded from \( 5 \times 10^{17} \text{ cm}^{-3} \) at the surface to \( 2 \times 10^{16} \text{ cm}^{-3} \) in the bulk. The breakdown voltage in this case is only 5.96 V, the current level at \( V_{in} = 2 \text{ V} \) (\( V_{CS} = 0 \text{ V} < V_T \)) is quite high at \( \approx 2.5 \mu A \), but further optimization should be possible. However the bulk breakdown mechanism is clearly visible in the figure.

7. PIMOS versus IMOS

Table 1 summarizes the main figures of merit of PIMOS compared to the IMOS, for this comparison the lateral IMOS is considered, as they are the most closely related in terms of technology and integration with CMOS.

The PIMOS fabrication is more closely related to CMOS and good reliability is obtained also at higher temperatures. The challenges for the PIMOS device are in terms of control of the subthreshold leakage current and the inherent short channel effects. The hysteresis effect can be an advantage for certain applications (memory), but control, or even elimination, of the hysteresis is required for logic applications. The IMOS, on the other hand, presents a lower leakage than a corresponding MOSFET and the scalability in terms of bias voltages is therefore limited by material parameters. The main challenges for the IMOS is in terms of processing technology and reliability. In planar devices operation is only assured for a few cycles, but this can be solved by the use of a vertical structure [6].

8. Applications

This section proposes and analyzes the exploitation of the PMOS transistor. First two DRAM architectures exploiting the hysteresis in \( I_d(V_{DS}) \), followed by a hysteretic inverter based on the hysteresis and abrupt switch in the \( I_d(V_{CS}) \) characteristics.

8.1. DRAM memory

It is possible to exploit the PIMOS as a one-transistor memory based on the \( I_d(V_{DS}) \) hysteresis shown in Fig. 17. In the hysteresis cycle is exploited to read “0” or “1” values after writing with low or high \( V_{DS} \) respectively. Structurally this resembles somewhat the capacitor-less 1T DRAM cell presented in [22,23], which relies on the storage of impact ionization generated charge in the floating body of a partially depleted SOI MOSFET. However, in the case of the PIMOS DRAM cell we do not rely on passive charge storage, but on the active hysteresis profile.

In the 1T DRAM cell, shown in the inset in Fig. 17, a transimpedance amplifier is used to achieve the current to voltage conversion. A high gain feedbacked OpAmp sets the \( V_{in} = V_{DS} \) biasing and the read-write operation, while \( V_{CS} = -0.5 \text{ V} \) during read and write.

Applying a negative \( V_{CS} = -2 \text{ V} \), during read can force the output down. However, since the low level of current (read and write “0”) is still pretty high due to the large \( V_{DS} \), the “0” level, do not go to zero, but only to an intermediate voltage level, this will give a high static power consumption for such a memory.

Therefore a preferable architecture incorporates an access device in a capacitor-less 1PIMOS-1T DRAM architecture, Fig. 18, uses an additional transistor \( T_2 \) acting as a common gate topology and decoupling the drain voltage of \( T_1 \) and the bit line (BL) node. This device is used to create a current comparator with very high output impedance. While its gate voltage allows to write, read and address the PIMOS memory cell. The memory state is read through the \( I_d \) of the storage transistors \( T_1 \), which corresponds to a PIMOS device.

![Fig. 17. Hysteresis in \( I_d(V_{CS}) \) characteristic for a device of \( L = 1.4 \mu m \) and width \( W = 40 \mu m \), \( V_{CS} = 0.5 \text{ V} \) and \( V_{DS} = 0 \text{ V} \), the slopes \( S_d \) take on a value ranging from 3–6 mV/dec. Inset shows the proposed memory configuration.](image-url)
with hysteresis. The cascode stage follows the drain current of $T_1$. The gate of the device $T_2$ is driven by a multi-level voltage ($V_{in}$) that is used to set the voltage level of $V_{DS1}$ to write, read and address the memory cell $T_1$. The output data is obtained by a current comparison at the BL node with a reference current $I_{ref}$ whose value is adjusted in the middle of the range of current between state “1” and “0”. This architecture has the advantage of shutting off current during hold, thus reducing power consumption, demonstration of memory functionality with full voltage swing is shown in Fig. 19. The hold state refers to the case, when the memory cell is decoupled, i.e., it is shut off by the access transistor, it does not refer to a storage of the memory state, the latter would correspond to an SRAM operation.

In the present embodiment off-chip discrete elements are used to implement the electronics circuitry. However, in the future it should be possible to implement these along the same silicon wire, as we have demonstrated it for a PIMOS-based inverter, thus allowing for true logic-on-wire.

8.2. Hysteretic PIMOS inverter and prospect for SRAM cell

We have recently demonstrated an N-PIMOS inverter consisting of a PIMOS input device and a pull-up NMOS load [24]. The inverter reproduces the abrupt switch and hysteresis from the $I_D(V_{DS})$ characteristics; the voltage transfer characteristic is shown in Fig. 20.

The PIMOS inverter characteristic is different from both that of a conventional CMOS and an IMOS based inverter, in that it incorporates three distinctly different regions of operation: (i) when the input PIMOS device is off, the pull-up network will pass the value of $V_{DD}$ to the output, (ii) when $V_{DS} > V_{DD}$ when the input exceeds the gate pull-up voltage, $V_{in} > V_{GPU}$, the PIMOS will pull down the output abruptly until it reaches the drain breakdown voltage, and (iii) beyond $V_{DBD}$ the device is still on, unlike an IMOS, it just works as a quasi-conventional short-channel MOSFET at high $V_{DS}$, after abrupt switching in $V_{GS}$ where the current $I_D$ is dictated by both MOSFET and bipolar contributions. So the MOSFET operation will continue to pull down the output until the point determined by the load network, i.e., a resistive divider in the case of an N-PIMOS.

The hysteretic VTC characteristic in Fig. 20 supports the basic idea of an SRAM cell made of a single inverter, especially because the hysteresis width can be optimized by the value of applied $V_{DS}$. However, the main drawback of such a memory cell is the high current consumption.

Future prospects concerns the demonstration of a complimentary PIMOS inverter to reduce the static power consumption, however for a complementary PIMOS inverter it should be possible to evacuate the impact ionization current, similarly to the case of an IMOS inverter [7], thus the inverter might be designed with a resistor at the output in which case the output voltage will depend on the value of $R_L$.

9. Conclusion

In the present work we have described the operation of the punch-through impact ionization MOSFET which presents both abrupt less-than-10 mV/dec on-off and off-on transitions and a hysteresis in the $I_D(V_{DS})$ and $I_D(V_{GS})$ characteristics. The devices show remarkably good temperature stability up to 125℃. We have analyzed the scalability for this device in terms of device length and doping density, which is ultimately limited by the acceptable leakage current, a graded channel doping profile can improve the device performance. Finally, we have proposed and experimentally evaluated a capacitor less DRAM based on the PIMOS $I_D(V_{DS})$ hysteresis as well as a hysteretic inverter.

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References


