A Novel Current Sensing Circuit for a Current-Mode Control CMOS DC-DC Buck Converter

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ABSTRACT

A novel on-chip current-sensing technique, which is suitable for a current-mode control CMOS DC-DC buck converter, is presented in this paper. The proposed current sensing circuit doesn’t need an op amp as a voltage mirror, and thus fewer transistors are need and lower power consumption is achieved. We use the TSMC 0.35μm 2P4M CMOS process to design and simulate the converter circuits. Simulation results show that accuracy of current-sensing for the proposed circuit is 98.2% and the core circuit’s power consumption is only 81.22mW. Under the same technology and the operating conditions, the performance of the proposed circuit is the best compared to the other circuits.

I. Introduction

In today’s consumer market, battery-operated portable electronic devices such as cellular phones, personal digital assistants (PDAs), and other palm-size devices are in great demand. Power management ICs, such as the highly efficient low-voltage switch-mode DC-DC converters, are mandatory in these devices for maximizing the system run time. In order to decrease the size and weight of these devices, miniaturization of the power modules is essential. For voltage conversion performed by custom-designed highly integrated converters with individual loads, the volume of the converters will typically be much smaller than the volume of all batteries required to achieve the equivalent extension of run time [1].

In addition, it is well-known that the current-mode control DC-DC buck converter takes the advantages of automatic over-current protection, better stability, better line regulation, and faster dynamic responses compared with the voltage-mode control [2]. It is used for over-current protection and current-mode feedback control. It can also be used in fuel gauge application for battery chargers. Many different current-sensing schemes have been developed and implemented to sense the inductor current [3-6]. Other approaches include the use of a series resistor, the on-resistance of the power MOSFET and even an integrator. However, these schemes have their limitations such as high power dissipation, process-dependence, difficulty in control and also high complexity of implementation. Therefore, an accurate current sensing circuit is necessary for all current-mode control switch-mode power converters (SMPC).

Therefore, a novel on-chip current-sensing circuit for current-mode control DC-DC buck converter in TSMC 0.35μm 2P4M CMOS process is proposed. The proposed circuit provides solutions to many problems of the existing current-sensing circuits. The existing current-sensing circuits are addressed in Section II. The operational principle of the proposed on-chip current-sensing circuit is described in Section III. The simulation and comparison results are included in Section IV. Finally, the summary is given in Section V.

II. Existing current-sensing circuits

The accuracy of the current-sensing circuit shown in Figure 1 [5] is mainly dependent on the voltage at VA and VB. In order to achieve a high accuracy, a two-stage cascode opamp with a floating class-AB output stage [7] is used to force the voltage at node A and node B to be the same.

Figure 1 The on-chip current-sensing circuit for current-mode control dc-dc buck converter [5]

Two current sources, I1 and I2, of small and equal magnitude pull the current from node V1 and V2. An output current Ip1, which flows through the power transistor MP1, is mirrored to the sense transistor MP2. Any change in V1 will force a similar change in V2 due to the virtual short-circuit provided by the operational amplifier. Thus, the drain-to-source voltage VDS of transistors MP1 and MP2 are almost the same, as well as their drain currents. However, the transistors MP1 and MP2 are scaled so that power transistor MP1 on the output side of the circuit has an aspect ratio much greater than that of transistor MP2 on the sensing side, for
example 2000:1. As a result, the current $i_{p2}$ on the sensing side is much smaller than, and proportional to the current $i_{p1}$ on the output side. The output sensing current $i_{sense}$, which passes through the internal resistor $R$, is the difference between the sensing current $i_{p2}$ flowing through the transistor $MP2$ and the current $i_2$ flowing through the small biasing current source. Therefore, the current $i_{sense}$ flowing through the internal resistor $R$ is proportional to and substantially much smaller than the current $i_{p1}$ flowing through the load.

For the current-mode buck converter application, the sensing voltage $V_{sense}$ is useful in the control feedback loop only during the ON-stage (the ramp up portion of the inductor current) [5]. Thus, only the signal from the power transistor $MP1$ during turn ON is useful, and therefore, the gate of the transistor $MP2$ is always coupled to ground. The switches $MS1$ and $MS2$ are used such that the node $V_A$ would not be shorted to the ground during the OFF-state of the switching cycle. As a result, there will not be a large current flowing through the sensing resistor $R$. In addition, the transistor $MR$ should always operate in the saturation region such that there is enough drain-to-source $V_{DS}$ drop across $MR$ and $V_{sense}$ will not go to $Vdd$ [5].

Leung et al. proposed another on-chip current-sensing circuit [6] as shown in Figure 2. The operational principle is similar to the one proposed by Lee [5]. But the circuit has fewer transistors, and the operational amplifier is a two-stage cascode opamp without floating class-AB output stage.

III. Proposed on-chip current-sensing circuit

Figure 3 shows the proposed current-sensing circuit, which can control the output voltage and manage the loading current of the DC-DC buck converter. Since the power PMOS $MP1$ is operated in the triode region, the drain current can be obtained as:

$$I_{p1} = \frac{1}{2} \mu_p C_{ox} \left( \frac{W}{L} \right)_{MP1} \left[ 2(V_{SD} - V_{TP}) - V_{SD}^2 \right]$$  \hspace{1cm} (1)

where $\mu_p$, $C_{ox}$, $W$, $L$, $V_{SD}$, $V_{TP}$ and $V_{SD}$ stands for effective channel mobility, gate oxide capacitance per unit area, channel width and length of $MP1$ transistor, source-gate voltage, threshold voltage, and source-drain voltage, respectively. The source-gate of the power PMOS $MP1$ is equal to those of the sensing PMOS $MPSEN$. Therefore, if the relationship of the aspect ratio between the sensing PMOS $MPSEN$ and the power PMOS $MP1$ is designed as $I:K$, the drain currents $i_{p1}$ and $i_{p1}/K$ of the power PMOS $MP1$ and sensing PMOS $MPSEN$ would have the following relationship:

$$I_{p2} = \frac{1}{2} \mu_p C_{ox} \left( \frac{W}{L} \right)_{MPSEN} \left[ 2(V_{SD} - V_{TP}) - V_{SD}^2 \right]$$  \hspace{1cm} (2)

$$K = \frac{I_{p1}}{i_{p2}} = \frac{\left( \frac{W}{L} \right)_{MP1}}{\left( \frac{W}{L} \right)_{MPSEN}}$$  \hspace{1cm} (3)

Figure 2 Another on-chip current-sensing circuit [6]

Figure 3 Proposed on-chip current sensing circuit for current-mode control dc-dc buck converter

Because the channel widths of NMOS $MN1$ and PMOS $MP1$ used as switches in a switching converter are very large to minimize the conduction power dissipation, it is necessary to use a driver circuit with large driving ability [8]. Beside the condition loss in the switching converter, the short-circuit power dissipation is also necessary to be consider. If we make the PMOS and NMOS devices not conduct at the same time, then the short-circuit power dissipation will be eliminated. We control the on and off time of the PMOS and NMOS by two clocks $CKP$ and $CKN$ which are shifted by a constant time and has a different duty cycle. Due to this method, these two transistors $MP1$ and $MN1$ will not conduct at the same time [9] as shown in Figure 4.
are obtained by passing CKin through the gate driver circuit. Figure 6 shows their waveforms. When the supply voltage is 5V, Figure 7 shows that the inductor peak current is 113mA at 200μsec. Figure 8 shows that the current of the Mscnp is 111μA at 200μsec. Since the ratio K is set to 1000, the accuracy of current-sensing is 98.2%. Figure 9 shows the voltage waveforms of VA and VB. The voltage of the VA and VB are almost the same. For comparison, the other circuits in [5,6] are also designed and simulated by using the same technology. The supply voltage, CKin, and the gate driver circuit and the same. We also utilized the same-size MP1, MN1, and off-chip inductor and capacitor. Comparisons of simulation results are summarized in Table I. The proposed circuit has the lowest average power consumption, the highest accuracy of current-sensing, and the lowest number of mosfet since it doesn't need an op amp to as a voltage mirror. The performance of the proposed circuit is the best compared to the other circuits.

Figure 5 illustrates a simplified structure of a current-mode control DC-DC buck converter. The converter is composed of a power stage and a feedback network. The power stage contains a switching element, which consists of the power PMOS and NMOS transistors, and an output filter. The output filter is composed of an inductor L and a filtering capacitor C. The output voltage is scaled down to bVo and compared with the reference voltage Vref before feeding into the compensator. The output of the compensator, compensation ramp and sensed inductor current signal will pass through the modulator and the digital control block to define the duty ratio d(t). The duty ration d(t) controls the on-time and off-time duration of the power transistors such that a negative feedback is achieved to regulate the output voltage Vo [2,7].

![Figure 5 Structure of a current-mode control DC-DC buck converter](image)

**IV. Simulation and Comparison Results**

We use the TSMC 0.35 μm 2p4m CMOS process to design and simulate the proposed on-chip current sensing circuit for the current-mode control DC-DC buck converter. CKin is 500KHz and the duty cycle is 50%. CKP and CKN
A novel on-chip current-sensing circuit for a current-mode control DC-DC buck converter has been described in this paper. The proposed circuit has the lowest average power consumption, the highest accuracy of current-sensing, and the lowest number of mosfet compared with the other circuits.

Simulation results show that accuracy of current-sensing for the proposed circuit is 98.2% and the core circuit’s power consumption is only 81.22mW.

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VII. References


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