Thermal noise analysis of switched-capacitor integrators with correlated double sampling

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SUMMARY

Correlated double-sampling (CDS) is widely used to suppress the effect of flicker noise in switched-capacitor (SC) circuits. Once the flicker noise is suppressed by CDS, the noise of the SC circuits is ultimately determined by the thermal noise. In this work, we develop a method to calculate the thermal noise in SC integrators as functions of a variety of circuit parameters such as capacitor size and switch resistance; this methodology is then applied to a CDS integrator as well as a conventional integrator. We found that for the CDS integration scheme, in order to avoid significantly increasing the noise power of the integrator, the size of the CDS capacitor should be comparable to that of the sampling capacitor. We also found that if the CDS capacitor is sufficiently large, the noise power of a CDS integrator is almost the same as that of a conventional integrator with the same sampling capacitor size. These findings are explained based on the bandwidth of the transfer functions.

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KEY WORDS: correlated double sampling; switched-capacitor integrator; thermal noise

1. INTRODUCTION

The switched-capacitor (SC) technique is popularly used in analog or mixed-signal CMOS integrated circuits [1, 2]. To suppress the effects of DC offset and the flicker noise of operational amplifiers (op-amps) in SC circuits, the correlated double-sampling (CDS) technique is widely adopted. The noise suppression characteristics of SC CDS circuits have been studied by several authors [3–6]. [3] analyzed CDS as a special case of auto-zeroing and reported frequency-dependent noise suppression characteristics of idealized CDS systems. [4, 5] developed a methodology to analyze the noise performance of CDS circuits and applied it to some popular integrator structures. However, [4, 5] focused on the charge transfer between switched capacitors and the correlation between the noise voltages, but did not provide the explicit noise transfer functions (TFs) from the noise sources to the noise voltages stored at the capacitors.

[7] investigated the effects of the capacitances, on-resistance of switches, and op-amp characteristics on the noise of SC integrators. However, analysis in [7] was limited to conventional SC integrators and did not include CDS integrators.

In this work, we present a thermal noise analysis of SC integrators, which can be applied to CDS integrators as well as to conventional integrators. Similar to the analysis conducted in [4, 5], our analysis is based on the noise charge transfer between switched capacitors. However, our analysis presents noise TFs that account for the effect of various circuit parameters, which should prove to be more useful in the design of SC integrators.

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The rest of the paper is organized as follows. In Section 2, we present an analysis of the noise power of SC integrators. We begin with a simple conventional integrator and proceed to the analysis of a CDS integrator. In Section 3, we verify the validity of the developed noise models with SpectreRF simulations and discuss the implications of our findings obtained from noise analysis of the integrators. In Section 4, we conclude the paper.

2. THEORY

Figures 1 (a) and (b) show the schematic diagrams of the conventional SC integrator [8] and the SC CDS integrator [9], respectively. The numbers beside the switches indicate the clock phases of the integrator (Φ₁ and Φ₂). \( V_f \) represents the input-referred noise of the op-amps and \( C_p \) represents the parasitic capacitance at the input of the op-amps. Operation of the circuits is based on the charge conservation principle and is well known. In both integrators, the input signal \( V_{IN} \) is sampled on the sampling capacitor \( C_1 \) in the sampling phase (Φ₁). In the integrating phase (Φ₂), the charge stored in \( C_1 \) is transferred to the integration capacitor \( C_2 \), resulting in integration with a gain of \( G = C_1/C_2 \).

In Figure 1 (a) of the conventional integrator, \( V_X \) is set to \( V_f \) in Φ₂, resulting in the integration of \( V_f \). However, in the CDS integrator, this noise integration is suppressed by sampling the noise in the sampling phase and subsequently subtracting it in the integration process. More specifically, in Figure 1 (b), \( V_f \) is stored on the CDS capacitor \( C_3 \) at the end of the Φ₁ phase. Therefore, if \( V_f \) does not change (or changes very slowly) between the Φ₁ and Φ₂ phases, as in the case of DC offset or low-frequency flicker noise, \( C_3 \) maintains a virtual ground at node \( Y \) during Φ₂; this makes complete charge transfer from \( C_1 \) to \( C_2 \) possible.

It should be noted that for proper operation of the circuits, the clock period \( T_s \) should be much longer than the various time constants of the circuits (\( RC \) or \( C/gm \)) so that complete charge transfer occurs. This condition is assumed throughout this paper.

2.1. Noise analysis of the conventional SC integrator

In this section, we analyze the noise performance of the conventional SC integrator. Figures 2 (a) and (b) show schematic diagrams of the conventional SC integrator in the Φ₁ and Φ₂ phases, respectively.

![Figure 1. Schematic diagrams of (a) a conventional SC integrator and (b) an SC CDS integrator.](image-url)
with the noise sources shown explicitly. \(V_{n1}, V_{n2}, V_{n4},\) and \(V_{n5}\) represent the thermal noises of the switches, and \(V_{n3}\) and \(V_{n6}\) represent the input-referred noises of the op-amp in the \(\Phi_1\) and \(\Phi_2\) phases, respectively. In this work, it is assumed that all thermal noise sources produce wide-band white noise with flat power spectral densities (PSDs) and that the thermal noises from different noise sources are mutually uncorrelated. \(R_1, R_2, R_4,\) and \(R_5\) represent the on-resistances of the switches. In this work, we assume that switch on-resistances are identical (i.e. \(R_1 = R_2 = R_4 = R_5 = R_{on}\)). The grey triangles represent the op-amp. In this work, we assume a single-stage op-amp with a DC gain of \(A = g_m R_{out}\), where \(g_m\) is the transconductance, \(R_{out}\) is the output resistance. \(C_4\) and \(C_5\) represent the load capacitances in the \(\Phi_1\) and \(\Phi_2\) phases, respectively. Note that usually \(C_4 > C_5\) because \(C_4\) includes contributions from the sampling capacitor of the next stage.

We begin our analysis by deriving the noise charge conservation relations. In transitions from \(\Phi_1\) to \(\Phi_2\), \(Q_{C1} + Q_{C2} - Q_{Cp}\) is preserved, where \(Q_{C1}\) represents the charge stored in capacitor \(C_1\). From this, we can obtain

\[
C_1 V_{C1}(k + 1/2) + C_2 V_{C2}(k + 1/2) - C_p V_{Cp}(k + 1/2) = C_1 V_{C1}(k) + C_2 V_{C2}(k) - C_p V_{Cp}(k), \tag{1}
\]

where \(V(k)\) and \(V(k+1/2)\) are voltages at the ends of the \(\Phi_1\) and \(\Phi_2\) phases of the \(k\)-th clock cycle, respectively. Similarly, in the transition from \(\Phi_2\) to \(\Phi_1\), \(Q_{C} - Q_{Cp}\) is preserved. From this, we obtain

\[
C_2 V_{C2}(k + 1) - C_p V_{Cp}(k + 1) = C_2 V_{C2}(k + 1/2) - C_p V_{Cp}(k + 1/2). \tag{2}
\]

By combining (1) and (2), we can obtain

\[
V_{C2}(k + 1) = \left(\frac{C_1}{C_2}\right) [V_{C1}(k) - V_{C1}(k + 1/2)] + \left(\frac{C_p}{C_2}\right) [V_{Cp}(k) - V_{Cp}(k + 1)] + V_{C2}(k). \tag{3}
\]
By summing (3) over $k$, we can obtain an explicit expression for $V_{C2}$.

$$V_{C2}(m) = \left(\frac{C_1}{C_2}\right)^{m-1} \sum_{k=0}^{m-1} [V_{C1}(k) - V_{C1}(k + 1/2)] - \left(\frac{C_p}{C_2}\right) V_{CP}(m). \quad (4)$$

From Figure 2 (a), we can obtain

$$V_{n,\text{out}}(m) = V_{CP}(m) + V_{C2}(m). \quad (5)$$

After substituting (4) into (5), we can express the output noise by

$$V_{n,\text{out}}(m) = \sum_{k=1}^{m} V_{n,\text{inref}}(k) + V_{n,\text{outref}}(m), \quad (6)$$

where

$$V_{n,\text{inref}}(k) = \left(\frac{C_1}{C_2}\right) [V_{C1}(k) - V_{C1}(k + 1/2)] \quad (7)$$

and

$$V_{n,\text{outref}}(m) = \left(1 - \frac{C_p}{C_2}\right) V_{CP}(m). \quad (8)$$

Following [7], we refer to $V_{n,\text{inref}}$ and $V_{n,\text{outref}}$ as the input-referred noise and the output-referred noise, respectively. $\Sigma V_{n,\text{inref}}$ represents the integration of the noise generated in the previous clock cycles, and $V_{n,\text{outref}}$ represents the noise produced in the current cycle. We found that contributions from the output-referred noise in the total noise power are negligible, which is in agreement with the findings in [4, 5, 7]. Therefore, we will focus on the input-referred noise for the remainder of this paper.

In this work, we assumed that the clock period is much longer than the various time-constants of the circuits and that the DC gain of the amplifier is large. Then, the $V_{n,\text{inref}}(k)$ values for different $k$ are uncorrelated to each other. Furthermore, $V_{C1}(k)$ and $V_{C1}(k + 1/2)$ in (7) are mutually uncorrelated. Using these, we can obtain an expression for the average power of the input-referred noise.

$$V_{n,\text{inref}}^2(k) = \left(\frac{C_1}{C_2}\right)^2 \left[ V_{C1}^2(k) + V_{C1}^2(k + 1/2) \right]. \quad (9)$$

By applying Parseval’s theorem, (9) can be expressed as

$$V_{n,\text{inref}}^2(k) = \left\{ \int |V_{n,\text{inref}}(f)|^2 df \right\} \left(\frac{C_1}{C_2}\right)^2 \left\{ \int \left|V_{C1}(k,f)\right|^2 + \left|V_{C1}(k + 1/2,f)\right|^2 \right\} df, \quad (10)$$

where $|V_{C1}(k,f)|^2$ and $|V_{C1}(k + 1/2,f)|^2$ are the PSDs of $V_{C1}(k)$ and $V_{C1}(k + 1/2)$, respectively.

The relationship between the noise voltages ($V_{n1} - V_{n6}$) and $|V_{C1}(k,f)|^2$ and $|V_{C1}(k + 1/2,f)|^2$ can be obtained by solving the nodal equations of the circuits shown in Figures 2 (a) and (b). Using these results, the PSD of the input-referred thermal noise can be expressed as

$$|V_{n,\text{inref}}(f)|^2 = \sum_{i=1}^{6} |F_i(f)|^2 |V_{n,i}(f)|^2, \quad (11)$$

where $|V_{n,i}(f)|^2 = 4kTR_i$ is the PSD of the thermal noise of $R_i$. Note that $R_3 = R_6 = 4/(3g_m)$ are the noise-equivalent resistances corresponding to $V_{n3}$ and $V_{n6}$ (the input-referred noise of the op-amp). $F_i(f)$ represents the TFs from $V_{n,i}(f)$ to $V_{n,\text{inref}}(f)$, which are obtained from nodal equations to be

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\[ F_1(s) = -F_2(s) = \frac{1}{1 + 2sR_{out}C_1}, \quad (12) \]

\[ F_3(s) = 0, \quad (13) \]

\[ F_4(s) = -F_5(s) = \frac{sR_{out} [C_1(C_5 + C_p) + GC_5C_p] + GC_p + C_1(1 + g_mR_{out})}{D(s)}, \quad (14) \]

\[ F_6(s) = -\frac{C_1g_mR_{out}}{D(s)}, \quad (15) \]

where

\[ D(s) = 2s^2R_{in}R_{out}C_1\left[C_1(C_5 + C_p) + GC_5C_p\right] + \left[R_{in}C_1^2 + C_1C_5(1 + G) + GC_5C_p\right] + \left(2R_{in}C_1\left[GC_p + C_1(1 + g_mR_{out})\right]\right] \]

\[ +G(C_1 + C_p) + C_1(1 + g_mR_{out}). \quad (16) \]

2.2. Noise analysis of the CDS integrator

Now, we calculate the noise of the SC CDS integrator following a procedure that is similar to the one used for the conventional integrator. In transitions from \( \Phi_1 \) to \( \Phi_2 \), \( Q_{C1} + Q_{C3} - Q_{Cp} \) and \( Q_{C3} + Q_{Cp} \) are preserved. From these, we can obtain

\[ C_1V_{C1}(k + 1/2) + C_3V_{C3}(k + 1/2) - C_pV_{Cp}(k + 1/2) = C_1V_{C1}(k) + C_3V_{C3}(k) - C_pV_{Cp}(k), \quad (17) \]

\[ C_3V_{C3}(k + 1/2) + C_pV_{Cp}(k + 1/2) = C_3V_{C3}(k) + C_pV_{Cp}(k). \quad (18) \]

In transitions from \( \Phi_2 \) to \( \Phi_1 \), \( Q_{C2} - Q_{C3} - Q_{Cp} \) is preserved; from this, we can obtain

\[ C_2V_{C2}(k + 1) - C_3V_{C3}(k + 1) - C_pV_{Cp}(k + 1) = C_2V_{C2}(k + 1/2) - C_3V_{C3}(k + 1/2) - C_pV_{Cp}(k + 1/2). \quad (19) \]

By substituting (17) and (18) into (19), we obtain

\[ C_2V_{C2}(k + 1) = C_2V_{C2}(k) + C_1[V_{C1}(k) - V_{C1}(k + 1/2)] + C_p[V_{Cp}(k + 1) + V_{Cp}(k + 1/2) - 2V_{Cp}(k)] + C_3V_{C3}(k + 1) - V_{C3}(k). \quad (20) \]

By summing (20) over \( k \), we can obtain an explicit expression of \( V_{C2} \).

\[ V_{C2}(m) = \left(\frac{C_1}{C_2}\right) \sum_{k=1}^{m-1} [V_{C1}(k) - V_{C1}(k + 1/2)] - \left(\frac{C_1}{C_2}\right) \sum_{k=1}^{m-1} [V_{Cp}(k) - V_{Cp}(k + 1/2)] + \left(\frac{C_1}{C_2}\right) V_{C3}(m) + \left(\frac{C_1}{C_2}\right) V_{Cp}(m). \quad (21) \]

From Figure 2 (a), we can obtain

\[ V_{OUT}(m) = V_{C2}(m) + i_{R3}(m)R_3 + V_{n3}(m) + V_{Cp}(m), \quad (22) \]

where \( i_{R3}(m) \) represents the current carried by \( R_3 \) at the end of the \( m \)-th \( \Phi_1 \) phase. Here, it was assumed that the output is sampled at the end of \( \Phi_1 \). After substituting (21) into (22), we can express the output noise as

\[ V_{n,\text{out}}(m) = \sum_{k=1}^{m-1} V_{n,\text{inref}}(k) + V_{n,\text{outref}}(m), \quad (23) \]

where \( V_{n,\text{inref}} \) is the input-referred noise, which is expressed by

\[
V_{n,\text{inref}}(k) \equiv (C_1/C_2)[V_{C1}(k) - V_{C1}(k + 1/2)] - \left( C_p/C_2 \right) [V_{Cp}(k) - V_{Cp}(k + 1/2)],
\]

(24)

and \( V_{n,\text{outref}} \) is the output-referred noise, which is expressed by

\[
V_{n,\text{outref}}(m) \equiv (C_3/C_2)V_{C3}(m) + (1 + C_p/C_2)V_{Cp}(m) + i_{B3}(m)R_3 + V_{n3}(m).
\]

(25)

In the conventional integrator, \( V_{C1}(k) \) and \( V_{Cp}(k) \) resulted from the noise in the \( \Phi_1 \) phase, and \( V_{C1}(k+1/2) \) and \( V_{Cp}(k+1/2) \) resulted from the noise in the \( \Phi_2 \) phase. However, in the CDS integrator, \( V_{C1}(k+1/2) \) resulted from both the noise in the \( \Phi_2 \) phase \( (V_{n5} - V_{n7}) \) and the noise in the \( \Phi_1 \) phase \( (V_{n1} - V_{n7}) \); this is because the noise sampled by \( C_3 \) in \( \Phi_1 \) is passed to the \( \Phi_2 \) phase. If we define \( V_{C11}(k+1/2) \) and \( V_{C12}(k+1/2) \) as the parts of \( V_{C1}(k+1/2) \) resulting from noise in the \( \Phi_1 \) and \( \Phi_2 \) phases, respectively, then (from charge conservation relations) we can obtain

\[
V_{C11}(k + 1/2) = V_{C3}(k) + \left( C_p/C_3 \right)V_{Cp}(k).
\]

(26)

Then, the input-referred noise of (23) can be expressed as

\[
V_{n,\text{inref}}(k) = \frac{C_1}{C_2} \left[ V_{C1}(k) - V_{C3}(k) - \left( \frac{C_p}{C_3} + \frac{C_p}{C_1} \right) V_{Cp}(k) \right] - \frac{C_1}{C_2} \left[ \frac{C_p}{C_1} V_{Cp}(k + 1/2) - V_{C12}(k + 1/2) \right].
\]

(27)

where the terms in the first pair of brackets on the right-hand side represent contributions by the noise of the \( \Phi_1 \) phase and the terms in the second pair of brackets represent contributions by the noise of the \( \Phi_2 \) phase.

As in the case of the conventional SC integrator, the relationship between noise sources \( (V_{n1} - V_{n7}) \) and \( V_{C1}(k) \), \( V_{Cp}(k) \), \( V_{C3}(k) \), \( V_{C12}(k+1/2) \), and \( V_{Cp}(k+1/2) \) in (27) can be obtained by solving the nodal equations of the circuits shown in Figures 3 (a) and (b). Then, the PSD of the input-referred noise can be expressed as

\[
|V_{n,\text{inref}}(f)|^2 \equiv \sum_{l=1}^{7} |H_l(f)|^2 \left| V_{n,l}(f) \right|^2,
\]

(28)

where \( |V_{n,l}(f)|^2 = 4k_B T R_l \) is the PSD of the thermal noise voltage from \( R_l \). Note that \( R_4 = R_7 = 4/(3g_m) \) are the noise-equivalent resistances corresponding to \( V_{n4} \) and \( V_{n7} \). \( H_l(f) \) is the TF from \( V_{n,l}(f) \) to \( V_{n,\text{inref}}(f) \), which can be expressed by

\[
H_1(s) = \{ s^2R_{on}^2C_4[ C_1 + 2C_3 + C_p ] \\
+ sR_{on}[1 + G(C_3 + C_p/C_1)C_4 + C_3 + C_p + g_m R_{on}(C_1 + C_3 + \{ C_1 + 2C_3 + C_p \}/A)] \\
+ g_m R_{on}[1 + \{ 1 + G(C_3 + C_p/C_1)/A \}/D_1(s) \}
\]

(29)

\[
H_2(s) = -\{ s^2R_{on}^2C_4C_p + s^2R_{on}^2[-C_1 + C_3 + C_p + C_3C_p(1 + G)/C_1]C_4 + C_3C_p(1 + g_m R_{on}/A)] \\
+ sR_{on}[C_3G(C_3 + C_p/C_1)/C_4 - g_m R_{on}(C_1 + C_3 - C_p - C_3C_p(1 + G)/C_1)/A] \\
+ C_3 + C_p + C_3C_p/C_1 + g_m R_{on}[G(C_3 + C_p + C_3C_p/C_1)/(C_1A)] /D_1(s),
\]

(30)

\[
H_3(s) = \{ s^3R_{on}^3C_4C_p(C_1 + C_3) \\
+ s^3R_{on}^3C_4[2C_1 + C_3 + 3C_p + C_p(C_3/C_1 + 2C_1/C_3) + g_m R_{on}C_p(C_1 + C_3)/A] \\
+ sR_{on}[1 + C_p(1/C_1 + 1/C_3) + g_m R_{on}(2C_1 + C_3 + 3C_p + C_p(C_3/C_1 + 2C_1/C_3))/A] \\
+ g_m R_{on}[1 + C_p(1/C_1 + 1/C_3)] /A /D_1(s),
\]

(31)
\[ H_4(s) = -g_mR_{on}\left[s^2R_{on}^2C_p(C_1 + C_3) + sR_{on}\left[2C_1 + C_3 + 3C_p + C_p(C_3/C_1 + 2C_1/C_3)\right]\right] + \left[1 + C_p(1/C_1 + 1/C_3)\right]/D_1(s), \] (32)

\[ H_5(s) = -\left\{sR_{on}C_3(1 + C_p/C_3) + g_mR_{on}\left[1 + (1 + C_p/C_3)/A\right]\right\}/D_2(s), \] (33)

\[ H_6(s) = -\left\{s^2R_{on}^2C_3C_p + sR_{on}\left[C_4 + C_5C_p(1/C_1 + 1/C_3) + g_mR_{on}C_p/A\right]\right\} + g_mR_{on}\left[1 + C_p(1/C_1 + 1/C_3)\right]/A}/D_2(s), \] (34)

and

\[ H_7(s) = g_mR_{on}\left[sR_{on}C_p + (1 + C_p/C_1 + C_p/C_3)\right]/D_2(s), \] (35)

where

\[ D_1(s) = s^4R_{on}^4C_1C_3C_4C_p + s^3R_{on}^3\left\{3C_1C_3 + 2C_1C_p + C_3C_p(1 + G)\right\}C_4 + C_1C_3C_p[1 + g_mR_{on}/A] \]

\[ + s^2R_{on}^2\left[2C_1 + 2C_3 + C_p + G(2C_3 + 2C_p + C_3C_p/C_1)\right]C_4 \]

\[ + C_1C_3(2 + g_mR_{on}) + C_p(2C_1 + C_3) \]

\[ + g_mR_{on}\left[3C_1C_3 + 2C_1C_p + C_3C_p(1 + G)\right]/A\} \]

\[ + sR_{on}\left[1 + G(C_3 + C_p)/C_1\right]C_4 + C_3 + C_p + g_mR_{on}(2C_1 + C_3) \]

\[ + g_mR_{on}\left[2C_1 + 2C_3 + C_p + G(2C_3 + 2C_p + 2C_3C_p/C_1)\right]/A\} \]

\[ + g_mR_{on}\left\{1 + \left[1 + G(C_3 + C_p)/C_1\right]/A\right\} \] (36)

and...
$D_2(s) = s^3 R_{on}^2 C_1 C_3 C_p + s^2 R_{on}^2 \{ [2C_1 + C_p (1 + G) + 2C_1 C_p / C_3] C_5 + C_1 C_p (1 + g_m R_{on} / A) \} + s R_{on} \{ [1 + C_p / C_3 + G (1 + C_p (1/C_1 + 1/C_3))] C_5 + C_1 + C_p + C_1 C_p / C_3 + g_m R_{on} [C_1 + (2C_1 + C_p (1 + G) + 2C_1 C_p / C_3) / A] \} + g_m R_{on} \{ [1 + C_p / C_3 + G (1 + C_p (1/C_1 + 1/C_3))] / A \} , \hspace{1cm} (37)$

where $A$ represents the open-loop gain of the op-amp ($g_m R_{out}$).

Finally, the total input-referred thermal noise power can be obtained by integrating (28), as follows.

$$V^2_{n, \text{in ref}} = 4k_BT \sum_{l=1}^{7} \left[ R_{l1} \int_{0}^{\infty} |F_l(f)|^2 df \right] . \hspace{1cm} (38)$$

### 3. SIMULATION RESULTS AND DISCUSSION

A CAD tool (SpectreRF) was used to corroborate the noise model that was developed in this work [10]. The parameters listed in Table I were used in the simulations and model calculations unless otherwise specified.

Figure 4 compares the input-referred noise powers of the conventional SC integrator calculated by our model (lines) with those obtained from the SpectreRF simulations (symbols). We can observe very good matching between the results of the simulations and the calculations.

Figure 5 compares the input-referred noise powers of the CDS integrator calculated by our model with those from simulations. Again, we obtain very close agreements between the results from the model calculations and the simulations. Furthermore, in Figure 5, we can observe that the noise power is predominantly determined by whichever capacitor is smaller (between $C_1$ and $C_3$). For example, when $C_3$ is very small, the thermal noise power is determined by $C_3$ and is inversely proportional to $C_3$.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Parameter</th>
<th>Value</th>
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<td>$C_3$</td>
<td>3.3 pF</td>
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Figure 4. Simulated and calculated input-referred noise power of the conventional SC integrator as a function of $C_1$ ($C_p = 0$, $G = 1$).
However, when $C_3$ is much larger than $C_1$, increasing $C_3$ further does not continue to reduce the noise. A rule of thumb is that $C_3$ should be larger than $C_1$ to maintain the $C_1$-limited noise power.

Figure 6 compares the input-referred noise power of the CDS integrator with that of the conventional integrator. From Figure 6, we can observe that when $C_3 << C_1$, the noise power of the CDS integrator is determined by $C_3$ and is larger than that of the conventional integrator. However, as $C_3$ is increased, the noise power of the CDS integrator is gradually reduced. When $C_3 >> C_1$, the noise power approaches that of the conventional integrator. This does not agree with the general belief that CDS integrators suffer from increased wideband thermal noise because the amplifier noise is sampled twice.

We found that this is caused by the difference in the bandwidths of the TFs. Figure 7 illustrates this by comparing the TFs from the CDS integrator and the conventional integrator. In Figure 7, $|H_4|$ and $|H_7|$ represent the TFs for the amplifier noise in $\Phi_1$ [i.e. $V_{n4}$ in Figure 3 (a)] and $\Phi_2$ [i.e. $V_{n7}$ in Figure 3 (b)] in the CDS integrator, respectively, and $|F_6|$ represents the TF for the amplifier noise in $\Phi_2$ in the conventional integrator [i.e. $V_{n6}$ in Figure 2 (b)]. Note that $H_4(s)$ and $H_7(s)$ are given as (32) and (35), respectively, and $F_6(s)$ is given as (15). Also note that we show only one TF for the conventional integrator because only the amplifier noise sampled in $\Phi_2$ contributes to the noise of the integrator. In Figure 7, we observe that when the noise frequency is low, $|H_4|$ and $|H_7|$ are identical and equal to $|F_6|$. Because the thermal noise in $\Phi_1$ and $\Phi_2$ are not correlated, we are tempted to conclude that the CDS

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Figure 5. Simulated and calculated input-referred noise power of the SC CDS integrator as a function of $C_3$ ($C_p=0$, $G=1$).

Figure 6. Calculated input-referred noise power of the SC CDS integrator and the conventional SC integrator for several values of $C_3$ as a function of $C_1$ ($C_p=0$, and $G=1$).
The integrator suffers from a two-fold increase in the noise power. However, because \(|H_4|\) has a much narrower bandwidth than \(|H_7|\) and \(|F_6|\), as shown in Figure 7, the total integrated noise power from \(V_{n4}\) is negligible compared to that from \(V_{n7}\). Therefore, the CDS integrator and the conventional integrator have nearly identical input-referred noise power if \(C_3\) is sufficiently large.

Next, we investigate the effect of the parasitic capacitance at the input of the op-amp (\(C_p\)). Figure 8 shows the input-referred noise power of the CDS integrator as functions of \(C_p\) for several values of \(C_3\). The lines represent the model-calculations and the symbols represent the SpectreRF simulations. We can observe very good matching between the simulations and the model calculations, which corroborates the validity of the developed model again. We also observe that an increase in \(C_p\) increases the noise power of the CDS integrator. This can be explained as follows. In CDS integrators, the difference between the noise charges stored at \(C_p\) in the \(\Phi_1\) and \(\Phi_2\) phases is transferred to \(C_2\) and then integrated; this is represented by the second pair of brackets in (27). Therefore, if \(C_p\) becomes larger, more charge is transferred to \(C_2\), and the noise power is increased. The increase in noise power caused by \(C_p\) is reduced when \(C_3\) is large because charge sharing between \(C_p\) and \(C_3\) decreases the amount of charge transferred to the integration capacitor. The effect of \(C_p\) in the CDS integrator is compared to that of \(C_p\) in the conventional integrator. (7) indicates that \(C_p\) does not affect the input-referred noise of a conventional integrator and our simulation results confirmed this (data not shown).

Figure 7. TFs of op-amp noise of the conventional integrator and CDS integrator (\(C_1 = 0.1\) pF, \(C_3 = 1\) pF, \(C_p = 0\), and \(G = 1\)).

Figure 8. Input-referred noise power of the SC CDS integrator for several values of \(C_3\) as function of \(C_p\) (\(C_1 = 3.3\) pF, and \(G = 1\)).
Figure 9 shows the input-referred noise power of the CDS integrator as a function of the transconductance of the op-amp ($g_m$) with the gain of the op-amp ($A$) fixed at 400. Note that $R_{out} = A/g_m$. In Figure 9, we observe that the noise power decreases very slowly as $g_m$ is increased. This can be explained as follows. When $g_m$ is increased, (1) the input-referred noise of the op-amp is reduced, which reduces the integrator noise, and (2) the bandwidths of the noise TFs are increased, which increases the integrator noise. The results of Figure 9 indicate that the effect of the former is slightly larger.

Figure 10 shows the input-referred noise power of the CDS integrator as a function of the op-amp gain ($A = g_m R_{out}$). Here, $R_{out}$ was varied while $g_m$ was fixed at 1 mA/V. We observe that the noise power is almost constant for $A > 200$, and when $A$ is lowered below 200, the noise power begins to shrink. However, the reduction is very modest and only about 0.5 dB even at $A = 10$. Furthermore, it should be noted that when the op-amp gain becomes too low, the integrator transfer function deviates from the ideal one [$= Gz^{-1}/(1 - z^{-1})$] severely. Also note that when $R_{out}$ is varied as in Figure 10, the open-loop bandwidth of the op-amp is affected ($1/R_{out}C_L$). However, the bandwidth of the feedback circuit employed by the integrator is limited by time-constants $C_L/g_m$ or $R_mC$ rather than the bandwidth of the op-amp itself.

In many designs, the total area allocated for the capacitors is limited. Therefore, it is worthwhile to study how we should divide the total available capacitance among capacitors $C_1$, $C_2$, and $C_3$ to minimize the noise power. Figure 11 (a) plots the noise power as a function of $C_3/C_1$ for several

![Figure 9. Calculated input-referred noise of the CDS integrator for several values of $C_3$ as a function of $g_m$ with a fixed op-amp gain ($A = 400$). $C_1 = 3.3 \text{ pF}$, $C_p = 0$, and $G = 1$.](image9)

![Figure 10. Calculated input-referred noise power of the CDS integrator as a function of op-amp gain for several values of $C_3$. $g_m$ is fixed (1 mA/V) while $R_{out}$ was varied ($C_1 = 3.3 \text{ pF}$, $C_p = 0$, and $G = 1$).](image10)
integrator gains \( G \) with the total capacitance fixed at 15 pF. We can observe that when \( G = 1 \), the optimum ratio of \( C_3/C_1 \) is close to one. However, when \( G \) is reduced to 0.1, the optimum ratio exceeds two. This is because reducing \( C_1 \) by \( \Delta C \) enables an increase in \( C_3 \) by \((1 + 1/G)\Delta C\). Therefore, when \( G \) is small, the increase in the noise power caused by using a somewhat smaller \( C_1 \) is more than offset by the reduction in the noise caused by a much larger \( C_3 \). This explanation is corroborated by Figure 11 (b), which plots the noise power when \( C_1 + C_3 \) is fixed at 10 pF. We can observe that the noise power is minimized when \( C_3/C_1 = 0.72 \), regardless of the integrator gain. This clearly shows that the gain itself does not tilt the balance between \( C_1 \) and \( C_3 \), if the size of \( C_2 \) is excluded from the optimization.

Finally, we discuss the usefulness of the noise models for the SC integrators that was developed in this work. Currently, the noise performance of discrete-time SC circuits (including the CDS integrators studied in this work) can be analyzed using CAD tools such as SpectreRF. In fact, we used SpectreRF in our work to verify the validity of the proposed model. However, noise calculations using these CAD tools take very long periods of time, which reduces the efficiency of design processes that rely solely on these tools. In contrast, our models enable designers to compare the effect of various parameters very efficiently, which makes our models helpful when designing circuits.

4. CONCLUSION

In this work, we studied the thermal noise of SC integrators and developed models to calculate the noise power for a given set of capacitances and other integrator parameters. To validate our models, we performed simulations using SpectreRF and found excellent matches between our simulations and model calculations.

We found that if the CDS capacitor is sufficiently large, the CDS integrator has the same input-referred noise power as a conventional integrator of the same sampling capacitor. This contradicts the common belief that CDS integrators suffer from an increase in their thermal noise. We found that this can be understood by considering the bandwidths of the noise TFs.

We also studied the allocation of capacitors among sampling capacitors and CDS capacitors, while accounting for the effect of the integrator gain; this can be helpful in the real world design of area-limited SC circuits. Our findings provide insight into the relationship between capacitor size and the noise of SC CDS integrators.

REFERENCES


