Input Current Control for Bridgeless PFC Converter without Sensing Current

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Abstract—The bridgeless power-factor-correction (PFC) converter possesses higher efficiency than the conventional boost-type PFC converter due to its reduced conduction voltage drop and conduction loss. The conventional multiloop control needs to sense the input current to yield the desired sinusoidal current waveform. This paper presents a control method for bridgeless PFC converter to provide sinusoidal current without sensing input current. The performance of the proposed method is demonstrated by the provided results with a 600W prototype.

I. INTRODUCTION

The use of power-electronics products increases in a wide diversity of applications: power supplies for microelectronics, household electric appliances, electronics ballasts, battery charging, motor drives, power conversion, etc. which also results in the rich current harmonics.

As shown in Fig. 1(a), the diode rectifier cascaded with the boost DC/DC converter is widely used to perform the desired power factor correction (PFC) function [1-2] including input current shaping and output voltage regulation. In addition, more and more papers focus on the converter efficiency.

To reduce the conduction drop in the current flowing path, many bridgeless circuits had been proposed to reduce the conduction loss and improve the efficiency. The bridgeless converter has drawn much attention in recent years due to its higher efficiency compared to the conventional single-phase boost-type rectifier. Due to common ground, the bridgeless PFC converters in Fig. 1(b) are wildly used in [3-5] where two switches have common ground.

However, totem-pole bridgeless PFC converter was used in [6] where two switches are connected to the same leg as shown in Fig. 1(c). This circuit is suitable for parallel operation. To reduce the common-mode voltage and EMI noise, two diodes are connected to the bridgeless PFC converters as shown in Fig. 1(d).

In [9], the interleaved scheme is introduced to improve the efficiency of the bridgeless PFC converter. For the step-down applications of dc voltage smaller than the peak of the AC-side voltage, some Cuk-based and Sepic-based PFC converters were proposed in [10-11].

The comparison of bridgeless PFC converter and the measured efficiency can be found in [12-13].

Fig. 1. (a) Conventional boost PFC converter; (b) Bridgeless PFC converter [3-5]; (c) totem-pole bridgeless PFC converter [6]; (d) semi-bridgeless PFC converter [7-8].
The bridgeless PFC converter in Fig. 1(b) can be controlled by the identical gate signal. For the totem-pole bridgeless PFC converter in Fig. 1(c), two complete gate signals are required. Phase-adjusted gate signals can be used in Fig. 1(b) [3] and Fig. 1(d) [7]. In [8], the phase-shifted gate signals are used to simplify the current sensing method.

Control of bridgeless converter for PFC operation using conventional linear average current control requires sensing of the input current. However, input current sensing is much difficult for the bridgeless PFC converter.

The passive current-sensing method reported in [14] requires three current-sensing transformers. These transformers are complicated control circuit design. In [3], input current control is formulated and performed based on the dc-rail current, which can be easily acquired by a series-sensing resistor or other dc current-sensing method. In this paper, a new control method is developed based on the current sensorless control method [15].

Some simulation and experimental results are provided to verify the proposed control method.

II. BRIDGELESS PFC CONVERTER

Fig. 2 shows the bridgeless PFC converter and the control loop. The resistor \( r_L \) is used to represent the inductor resistance. The load resistor \( R_L \) is connected across the output voltage \( V_o \).

Both the input voltage \( v_i \) and the output voltage \( V_o \) are sensed and they are feedback to the duty signal generator. The outputs of the duty signal generator are the duty signal \( d(t) \) and the sign signal \( \text{sign}(v_i) \) of the input voltage.

Then, by the switching signal generator, two switching signals \( G_A \) and \( G_B \) are generated according to the following two equations.

\[
G_A = \text{sign}(v_i) \cdot d(t) \quad (1)
\]

\[
G_B = \text{sign}(v_i) \cdot d(t) \quad (2)
\]

where the sign function \( \text{sign}(\cdot) \) is defined as

\[
\text{sign}(x) = \begin{cases} 1, & \text{when } x \geq 0 \\ 0, & \text{when } x < 0 \end{cases}
\]

and the complete signal \( \text{sign}() \) of the sign signal \( \text{sign}() \) is defined as \( \text{sign}(\cdot)=1-\text{sign}(\cdot) \).

The following study is divided into positive input voltage and negative input voltage.

Positive half-period \( v_i > 0, \text{sign}(v_i) = 1 \)

When the input voltage is positive \( v_i > 0, \text{sign}(v_i) = 1 \), the gate signal is equal to the duty signal \( G_A = d(t) \) and the other gate signal is always equal to zero \( G_B = 0 \). That is, the switch \( T_B \) always blocks according to (1)-(3). The circuit at duty signal \( d(t) = 1 \) and \( d(t) = 0 \) are plotted in Fig. 3(a) and Fig. 3(b), respectively. The inductor voltage \( v_L \) can be expressed as

\[
v_L = v_i - V_F - r_L i_s \quad \text{when } d(t) = 1 \quad (4)
\]

\[
v_L = v_i - V_F - r_L i_s - V_o \quad \text{when } d(t) = 0 \quad (5)
\]

where \( V_F \) is assumed to be equal to the total voltage drop across the diode and the semiconductor switch.

Combining (4) and (5) by the average duty signal \( \langle d \rangle_{T_i} \), the average inductor voltage \( \langle v_L \rangle_{T_i} \) within the switching period \( T_i \) in positive half-period can be expressed as

\[
\langle v_L \rangle_{T_i} = v_i - V_F - r_L i_s - \langle d \rangle_{T_i} W_o
\]

Negative half-period \( v_i < 0, \text{sign}(v_i) = 0 \)

When the input voltage is less than zero \( v_i < 0, \text{sign}(v_i) = 0 \), the gate signal is zero and the other switching signal \( G_B = d(t) \). It means that the switch \( T_A \) always blocks in this half period. The conducting path at \( d(t) = 1 \) and \( d(t) = 0 \) are plotted in Fig. 3(a) and Fig. 3(b), respectively.
respectively. Therefore, the inductor voltage $v_L$ can be represented as

$$v_L = v_s + V_F - r_L i_s$$  \hspace{1cm} (7)$$

$$v_L = v_s + V_F - r_L i_s + V_o$$ \hspace{1cm} (8)

Similarly, integrating (7) and (8) by the average duty signal $\langle d \rangle_{T_s}$, the average inductor voltage $\langle v_L \rangle_{T_s}$ in negative half-period can be expressed as

$$\langle v_L \rangle_{T_s} = v_s + V_F - r_L i_s + (1 - \langle d \rangle_{T_s}) V_o$$ \hspace{1cm} (9)$$

where $\text{sign}(v_s) = 0$.

**Single-Switch Model**

By introducing the sign signal $\text{sign}(v_s)$, two average inductor voltages in (6) and (9) can be combined to become

$$\langle v_L \rangle_{T_s} = v_s + V_F - (2 \text{sign}(v_s) - 1) W_F - r_L i_s - (2 \text{sign}(v_s) - 1) (1 - \langle d \rangle_{T_s}) W_o$$ \hspace{1cm} (10)$$

Substituting the voltage sign signal $\text{sign}(v_s)$ with $(v_s + \sqrt{|v_s|})/(2|v_s|)$ from (3), the derived single-switch model can be simplified to

$$\langle v_L \rangle_{T_s} = v_s + \frac{v_s}{|v_s|} V_F - r_L i_s - \frac{v_s}{|v_s|} (1 - \langle d \rangle_{T_s}) W_o$$ \hspace{1cm} (11)$$

Fig. 5 shows the single-switch model of the bridgeless PFC converter.

**III. THE PROPOSED CONTROL METHOD**

The proposed control method is plotted in Fig. 6 where the duty signal $d(t)$ is obtained from the comparison of the control signal $v_{cont}$ and the triangular signal $v_{tri}$.

The output of the voltage control loop is the voltage amplitude signal $\hat{V}_L$. The zero-crossing points of input voltage are detected in order to generate two synchronized signals $s_1(t)$ and $s_2(t)$ by the look-up table. With the sinusoidal input voltage $v_s = \hat{V}_s \sin(\omega t)$, both synchronized signals $s_1$ and $s_2$ can be expressed as

$$s_1(t) = (2 \text{sign}(v_s) - 1) \cos(\omega t)$$ \hspace{1cm} (12)$$

$$s_2(t) = \sin(\omega t)$$ \hspace{1cm} (13)$$

Then, the control signal $v_{cont}$ is generated by

$$v_{cont} = \frac{1}{V_o} \left[ v_s - V_F - \frac{\hat{V}_L}{\omega L} (s_1(t) + r_L s_2(t)) \right]$$ \hspace{1cm} (14)$$

Due to the comparison with the control signal $v_{cont}$ and the unit triangular signal $v_{tri}$ varying between 0 and 1, the average value $\langle d \rangle_{T_s}$ of the duty signal $d(t)$ can be expressed as $\langle d \rangle_{T_s} = 1 - v_{cont}$ (i.e. $1 - \langle d \rangle_{T_s} = v_{cont}$). Additionally, substituting (14) into (11) yields the equivalent average inductor voltage

$$\langle v_L \rangle_{T_s} = \hat{V}_L \cos(\omega t)$$ \hspace{1cm} (15)$$

From the average inductor voltage in (15), the average input current must be

$$\bar{I}_s = \bar{I}_L = \frac{\hat{V}_L}{\omega L} \sin(\omega t) = \hat{I}_L \sin(\omega t)$$ \hspace{1cm} (16)$$

and is in phase with the input voltage $v_s$.

It is noted that the yielded average power is

$$P = \frac{\hat{V}_L \bar{I}_s}{2} = \frac{\hat{V}_L \hat{I}_s}{2 \omega L}$$ \hspace{1cm} (17)$$

and the average power $P$ is proportional to the voltage controller output $\hat{V}_L$. Therefore, the simple PI-type voltage controller can be included to the voltage controller to regulate the output voltage. And from (16), sinusoidal input current can also be obtained.
IV. Simulations

To validate the proposed current control, some simulations are presented. Table I shows the parameters of bridgeless PFC converter.

<table>
<thead>
<tr>
<th>Table I. The parameters of bridgeless PFC converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
</tr>
<tr>
<td>Output voltage</td>
</tr>
<tr>
<td>Inductor</td>
</tr>
<tr>
<td>ESR of the inductor</td>
</tr>
<tr>
<td>The sum of conduction voltage</td>
</tr>
<tr>
<td>Carrier frequency</td>
</tr>
<tr>
<td>Capacitor</td>
</tr>
</tbody>
</table>

Fig. 7 shows the simulated waveforms at various powers. From Fig. 7, the input voltages are in phase with the corresponded input currents. Furthermore, the output voltages are kept at 200V.

![Fig. 7. Simulated waveforms at (a) 200W; (b) 600W.](image)

Fig. 8 is simulated waveforms at 400W. From Fig. 8, only the gate signal GA switches when input voltage is positive. And only the gate signal GB switches during the negative input voltage. Two synchronized signals \( s_1 \) and \( s_2 \) are as shown in equations (11) and (12).

Simulated waveforms during load change from 400W to 600W are shown in Fig. 9. The output voltage drop to 194V during load change and it returns to 200V after one period of input voltage.

![Fig. 8. Simulated waveforms at 400W.](image)

![Fig. 9. Simulated waveforms during load change from 400W to 600W.](image)

Fig. 10 shows the simulated waveforms at various powers. From Fig. 7, the input voltages are in phase with the corresponded input currents. Furthermore, the output voltages are kept at 200V.

![Fig. 10. Implementation of the proposed control.](image)

The input current harmonics of the waveforms in Fig. 11 are listed in Table II where the limitations for the Class D in IEC-61000-3-2 standard are also provided for comparison. In the experiment, the yielded input current harmonics are below the IEC-61000-3-2 standard.
Table II. Harmonics of experimental results

<table>
<thead>
<tr>
<th>Harmonics</th>
<th>Class A</th>
<th>Class D 200W</th>
<th>Fig. 11(a)</th>
<th>Class D 400W</th>
<th>Fig. 11(b)</th>
<th>Class D 600W</th>
<th>Fig. 11(c)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fundamental</td>
<td>X</td>
<td>1.7616A</td>
<td>3.4403A</td>
<td>X</td>
<td>5.2297A</td>
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<td></td>
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<tr>
<td>3rd</td>
<td>2.3A</td>
<td>0.68A</td>
<td>1.36A</td>
<td>0.2844A</td>
<td>2.04A</td>
<td>0.5743A</td>
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<td>5th</td>
<td>1.14A</td>
<td>0.38A</td>
<td>0.76A</td>
<td>0.0389A</td>
<td>1.14A</td>
<td>0.0844A</td>
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</tr>
<tr>
<td>7th</td>
<td>0.77A</td>
<td>0.2A</td>
<td>0.4A</td>
<td>0.0368A</td>
<td>0.6A</td>
<td>0.0520A</td>
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<tr>
<td>9th</td>
<td>0.4A</td>
<td>0.1A</td>
<td>0.2A</td>
<td>0.0258A</td>
<td>0.3A</td>
<td>0.0338A</td>
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<tr>
<td>11th</td>
<td>0.33A</td>
<td>0.07A</td>
<td>0.14A</td>
<td>0.0251A</td>
<td>0.21A</td>
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<tr>
<td>13th</td>
<td>0.21A</td>
<td>0.0592A</td>
<td>0.1184A</td>
<td>0.0190A</td>
<td>0.1776A</td>
<td>0.0158A</td>
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<tr>
<td>15th</td>
<td>0.15A</td>
<td>0.0513A</td>
<td>0.1027A</td>
<td>0.0209A</td>
<td>0.154A</td>
<td>0.0139A</td>
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<tr>
<td>17th</td>
<td>0.132A</td>
<td>0.0453A</td>
<td>0.0906A</td>
<td>0.0157A</td>
<td>0.1359A</td>
<td>0.0111A</td>
<td></td>
</tr>
<tr>
<td>19th</td>
<td>0.118A</td>
<td>0.0405A</td>
<td>0.0811A</td>
<td>0.0133A</td>
<td>0.1216A</td>
<td>0.0085A</td>
<td></td>
</tr>
<tr>
<td>THD</td>
<td>11.27%</td>
<td>8.8%</td>
<td>11.41%</td>
<td>8.8%</td>
<td>11.41%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

To evaluate the transient response, the experimental results during load change from 400W to 600W are shown in Fig. 12. After the change of the load, the output voltage is well regulated to the desired voltage 200V.

VI. CONCLUSIONS

This paper proposed a current method which is implemented by FPGA-based system to control the bridgeless PFC converter. The proposed current method does not need to sense the input current. The control method can be extended to the boost-type PFC converter without sensing inout current. From simulations and experimented results, the proposed current method can work well at various power.

REFERENCES

[8] Musavi, F.; Eberle, W.; Dunford, W.G. "A Phase-Shifted Gating Technique Wi...


