Influence of Phase-Locked Loop on Input Admittance of Three-Phase Voltage-Source Converters

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Abstract—A regulated power converter can cause instability issues at its terminals with its input filter or the source. The Generalized Nyquist stability Criterion (GNC), when applied to the product of the source impedance and load admittance in the dq frame, can be used to analyze the stability of balanced three-phase ac systems. This paper presents the influence of the Phase-Locked Loop (PLL) on the input admittance of three-phase Voltage-Source Converters (VSC) for open loop, current-feedback and voltage feedback control conditions. Analytical results show that the PLL introduces a parallel admittance to the open loop admittance of the VSC, and that the current and voltage control loop have additional effects on it. Both simulation and experimental results are presented to verify this analysis. The possible instability due to different PLL design is also shown.

Index Terms—Phase-locked loop (PLL), voltage source converters, grid-tied inverter, active front end, admittance, stability, generalized Nyquist stability criterion (GNC)

I. INTRODUCTION

Controlled power electronic converters are constant power loads that feature negative small-signal input impedance. The increase of constant power loads in a system can hence produce small-signal oscillations and even instability. For three-phase balanced ac systems, the Generalized Nyquist stability Criterion (GNC)[1][2], which uses the source impedance and load admittance in the dq frame to predict stability at ac interface[3][4][5], is an effective method. When the source impedance is the same, changing of load admittance can potentially cause instability. This paper studies the impact of the Phase-Locked Loop (PLL) on the input admittance of three-phase Voltage-Source Converters (VSC). These converters are widely used as grid-tied inverters or active front end for motor drives. The impedance shaping of three-phase, grid-tied VSCs including PLL and current feedback control has been presented in [6], but the impedance was defined in the phase domain, and the paper is not focusing on PLL. Two dq domains, namely the converter and system domains were used in [7] to analyze the impact of the PLL on the input admittance of VSCs. This paper borrows this concept, expanding it to show that the PLL acts as bridge, through which, small-signal perturbations in the system voltage propagate to the duty ratio in both the system and converter domains as shown in Fig. 1, which has not been discussed in [7]. This effect further influences the VSC input admittance. Analytical results show that the PLL introduces a parallel admittance to the open loop admittance of the VSC, and when current and voltage feedback control are applied, they have additional effects on it. Experimental results are presented to verify the analysis. Changing of load converter input admittance could potentially cause instability issue as shown in [3]. This paper also shows an instable case caused by increasing PLL bandwidth with certain source. By applying GNC to the source impedance and load admittance, the instability can be predicted.

![Fig. 1. Influence of PLL on VSC input admittance](image)

II. VSC INPUT ADMITTANCE INCLUDING PLL

A. Small signal propagation path through PLL

To analyze the impact of PLL on the input admittance of VSC, we first define two dq domains. One is the system dq

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domain that uses the ac source angle for transformation from abc frame to dq frame. The other one is the converter dq domain. Converter senses ac source voltage and uses PLL to track the angle of the ac source. The output angle of PLL is then used for dq transformation inside converter. In steady state, converter dq frame is aligned with system dq frame. When there is perturbation on the ac source voltage the perturbation will propagate to PLL output angle. Since PLL is a bridge that VSC input voltage perturbation can pass through it and introduce perturbation on input current, the average model of power stage is in system dq domain, feedback control is in converter dq domain to control the power stage, the perturbation will further propagate to system abc domain duty ratio through PLL output angle, finally to the VSC input current in system dq domain. Through this analysis, the conclusion can be drawn that PLL dynamic will influence VSC input admittance.

Fig. 2 shows the average signal model of VSC with PLL and feedback control. Notice that, the average model of power stage is in system dq domain, feedback control is in converter dq domain. Between the two domains, signals are transformed by using rotation matrix $T_\theta$ as shown in (1) and (2) The angle $\theta$ is the output of PLL. It represents the phase difference between the two domains.

$$\ddot{d} = T_\theta \ddot{\theta}, \quad \ddot{\theta} = T_\theta \ddot{\theta}$$

$$T_\theta = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix}$$

To derive the transfer function matrices for power stage, one can use the small signal model shown in Fig. 4. For example, in order to derive open loop input admittance $Y_{in}$, one can force small signal perturbation from system duty ratio to be zero as shown in Fig. 4 and solve the circuit. The open loop impedance $Z_{in}$ expression is shown in (3) by doing matrix inverse one can get $Y_{in}$.

$$Z_{in} = \begin{bmatrix} \frac{R}{RCs + 1} & D_1^2 + 3LC_s \\ \frac{R}{RCs + 1} & D_1D_2 + 3LC_s \end{bmatrix} \begin{bmatrix} \frac{R}{RCs + 1} & D_1^2 + 3LC_s \\ \frac{R}{RCs + 1} & D_1D_2 + 3LC_s \end{bmatrix}$$

In order to derive $G_{PLL}^d$ and $G_{PLL}^i$, transfer function from system voltage to PLL output angle should be derived first. In

**B. Input admittance of VSC including PLL**

To make the analysis of VSC input admittance simple, the transfer function matrices flow chart, shown in Fig. 3, is developed to represent the circuit shown in Fig. 2. $G_{vl}^d$ is the transfer function matrix from duty ratio to output dc voltage; $G_{ve}^d$ is the transfer function matrix from source voltage to output dc voltage; $G_{vl}^i$ is the transfer function matrix from duty ratio to boost inductor current; $Y_{in}$ is the open loop input admittance. To represent the effect of PLL, $G_{PLL}^d$ and $G_{PLL}^i$ are added. Perturbation from system voltage spreads to system domain duty ratio through $G_{PLL}^d$; and to converter domain boost inductor current through $G_{PLL}^i$.
steady state, duty ratio, voltage and current vectors in converter domain are equal to the corresponding vectors in system domain as shown in (4).

\[
\vec{D'} = \vec{D}, \quad \vec{V'} = \vec{V}, \quad \vec{I'} = \vec{I}.
\] (4)

One can say that the angle between the vectors in converter domain and the vectors in system domain is 0, using the rotation matrix \( T \) in (5) can be written down.

\[
\vec{V'} = \begin{bmatrix} \cos(0) & \sin(0) \\ -\sin(0) & \cos(0) \end{bmatrix} \vec{V},
\] (5)

Small signal perturbation can be added to (5) to get (6).

\[
\begin{bmatrix} V'_d + \tilde{V} \\ V'_q + \tilde{V}_q \end{bmatrix} = \begin{bmatrix} \cos(0 + \tilde{\theta}) & \sin(0 + \tilde{\theta}) \\ -\sin(0 + \tilde{\theta}) & \cos(0 + \tilde{\theta}) \end{bmatrix} \begin{bmatrix} V'_d + \tilde{V}_d \\ V'_q + \tilde{V}_q \end{bmatrix}
\] (6)

By doing approximation of trigonometric functions, and cancel the steady state values relationship between converter domain voltage, system domain voltage and PLL output angle can be derived as shown in (7) and (8).

\[
\begin{bmatrix} V'_d + \tilde{V}_d \\ V'_q + \tilde{V}_q \end{bmatrix} = \begin{bmatrix} 1 & \tilde{\theta} \\ -\tilde{\theta} & 1 \end{bmatrix} \begin{bmatrix} V'_d + \tilde{V}_d \\ V'_q + \tilde{V}_q \end{bmatrix}
\] (7)

\[
\begin{bmatrix} \tilde{V}_d \\ \tilde{V}_q \end{bmatrix} = \begin{bmatrix} \tilde{V}_d + V'_d \tilde{\theta} \\ -V'_q \tilde{\theta} + \tilde{V}_q \end{bmatrix}
\] (8)

Recall that PLL output angle is:

\[
\tilde{\theta} = \tilde{V}_q \cdot tf_{PLL} \cdot \frac{1}{s}
\] (9)

Substitute (9) to (8), (10) shows the equation represent the relation between PLL output angle and system domain \( q \) channel voltage.

\[
\tilde{\theta} = \frac{tf_{PLL}}{s + V'_q tf_{PLL}} \tilde{V}_q
\] (10)

Define \( G_{PLL} \) as (11).

\[
G_{PLL} = \frac{tf_{PLL}}{s + V'_q tf_{PLL}}
\] (11)

For duty ratio, similar small signal analysis can be done. (12) shows that duty ratio in converter domain is the vector in system domain plus additional term related to system domain voltage.

\[
\begin{bmatrix} \tilde{d}_d \\ \tilde{d}_q \end{bmatrix} = \begin{bmatrix} 0 & D'_d G_{PLL} \\ 0 & -D'_q G_{PLL} \end{bmatrix} \begin{bmatrix} \tilde{V}_d \\ \tilde{V}_q \end{bmatrix} + \begin{bmatrix} \tilde{d}_d \\ \tilde{d}_q \end{bmatrix}
\] (12)

Then, \( G_{PLL}^d \) is defined as (13).

\[
G_{PLL}^d = \begin{bmatrix} 0 & -D'_d G_{PLL} \\ 0 & D'_q G_{PLL} \end{bmatrix}
\] (13)

Similar equation can be derived for boost inductor current as shown in (14).

\[
\begin{bmatrix} \tilde{i}_d \\ \tilde{i}_q \end{bmatrix} = \begin{bmatrix} 0 & I'_r G_{PLL} \\ 0 & -I'_r G_{PLL} \end{bmatrix} \begin{bmatrix} \tilde{V}_d \\ \tilde{V}_q \end{bmatrix} + \begin{bmatrix} \tilde{i}_d \\ \tilde{i}_q \end{bmatrix}
\] (14)

\( G_{PLL}^i \) is defined as (15).

\[
G_{PLL}^i = \begin{bmatrix} 0 & I'_r G_{PLL} \\ 0 & -I'_r G_{PLL} \end{bmatrix}
\] (15)

After every transfer function matrices are derived, solve the equations represented by Fig. 3 to get VSC input admittance with PLL as Fig. 6.

\[
Y_{in_{PLL}} = Y_{in} + G_{PLL} G_{in} G_{PLL}^d K_r
\] (16)

Define \( Y_{PLL,0} \) as the parallel admittance to the open loop admittance \( Y_{in} \) due to PLL effect as shown in (17).

\[
Y_{PLL,0} = G_{in} G_{in} G_{PLL}^d K_r
\] (17)
To verify the derivation shown above, average model simulation is carried out to compare with the analytical results. Table I shows the parameters.

### Table I. Parameters for Simulation and Calculation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tr>
<td>$V_{dc}$ (V)</td>
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<tr>
<td>$V_{s_d}$ (V)</td>
<td>99.6</td>
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<tr>
<td>$V_{s_q}$ (V)</td>
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<td>$f$ (Hz)</td>
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<tr>
<td>$C$ (μF)</td>
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<tr>
<td>$L$ (μH)</td>
<td>500</td>
</tr>
<tr>
<td>$R_s$ (mΩ)</td>
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</tr>
<tr>
<td>$R$ (Ω)</td>
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<td>$D_s^d$</td>
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<tr>
<td>$D_s^q$</td>
<td>-0.0382</td>
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</table>

PLL bandwidth is 100Hz. The transfer function of the PLL low pass filter is:

$$f_{PLL} = \frac{8.921s + 3964}{s}$$  \hspace{1cm} (18)

The Bode plot of $f_{PLL}$ is shown in Fig. 5.

Fig. 6 shows the comparison between the analytical calculations presented (red curve) and average model simulations (dotted light blue curve), where it is clear that they match each other. In addition, the open loop admittance $Y_{in}$ (dotted dark blue curve) and additional admittance caused by PLL $Y_{PLL,o}$ (dotted green curve) are shown in this figure. As seen, because the PLL output angle is only influenced by the $q$-axis voltage, $Y_{PLL,o}$ does not have a value on the $Y_{dd}$ and $Y_{dq}$ elements. Within the PLL bandwidth, the phase of $dq$ and $qq$ elements of $Y_{PLL,o}$ have almost a 180° difference from the corresponding elements of the open loop admittance $Y_{in}$. This means that the $Y_{dq}$ and $Y_{qq}$ elements of $Y_{in,ol,PLL}$ are reduced.

### III. VSC Input Admittance with PLL and Feedback Control

#### A. Input admittance with current feedback control

To include the current controller to the transfer function matrix flow chart, current controller matrix $G_{ci}$ and decoupling control term matrix $G_{dei}$ are introduced as shown in Fig. 7.

Solving the equation represented by Fig. 7, VSC input admittance with PLL and current feedback control is (19).

$$Y_{in,PLL} = [I + \begin{bmatrix} G_{d} & G_{q} \\ \end{bmatrix} \begin{bmatrix} -G_{d} + G_{q} \end{bmatrix} K_i]^{-1} \cdot \begin{bmatrix} Y_{m} - G_{d} \end{bmatrix} G_{d} \begin{bmatrix} \left[\begin{bmatrix} -G_{d} + G_{q} \end{bmatrix} G_{d} - G_{PLL} K_i \right] \end{bmatrix}^{-1}$$  \hspace{1cm} (19)

To verify (19), average model simulation is carried out to compare with the analytical results including the current feedback control. Table II shows the parameters for current controller used for comparison.

### Table II. Parameters of Current Controller

<table>
<thead>
<tr>
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<tr>
<td>$I_{dref}$ (V)</td>
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<td>$I_{qref}$ (V)</td>
<td>0.0257</td>
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<td>$K_{pi}$</td>
<td>3141.6</td>
</tr>
<tr>
<td>$K_{ii}$</td>
<td>628.3185</td>
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</table>

Fig. 8 shows the comparison between the simulation results (red curve) and analytical expression results (dotted blue curve), they are matching.

Fig. 9 shows the comparison of VSC input admittance with different PLL bandwidth and current feedback control.
Fig. 9 shows the effect of the current loop and the PLL on the VSC input admittance. Clearly, the resonance shown by the open loop admittance is smoothed out by the current loop controller. Similarly to the open loop case, PLL only affects the $Y_{dq}$ and $Y_{qq}$ elements. In consequence, changes in the PLL bandwidth only influence the VSC admittance on its $Y_{dq}$ and $Y_{qq}$ elements, where a faster PLL will yield lower admittances within its bandwidth. A VSC, which input phase-to-neutral voltage is 57.5 V rms line frequency is 400 Hz, dc voltage is 270 V, with current loop controller in the $dq$ frame, which bandwidth is 1kHz, and different PLL bandwidths has been used as experimental validation for the previous analysis. The $dq$ frame impedance analyzer developed in [5] was used for measurements. As shown in Fig. 10, the PLL only varies its $Y_{dq}$ and $Y_{qq}$ elements under faster PLL designs (red curve), yielding lower admittance values compared to slower cases (blue curve). The experimental results validated the analysis discussed before.

Table III shows the parameters for voltage controller.

<table>
<thead>
<tr>
<th>Table III. Parameters of Voltage Controller</th>
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<tbody>
<tr>
<td>$V_{dref}$ (V)</td>
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<tr>
<td>$I_{qref}$ (V)</td>
</tr>
<tr>
<td>$K_{pv}$</td>
</tr>
<tr>
<td>$K_{iv}$</td>
</tr>
</tbody>
</table>

Solving the equation represented by Fig. 11, VSC input admittance with PLL and current and voltage feedback control is (20).

$$Y_{incl. PLL} = \left( I + G_{dd}(I + G_{di}G_{de}G_{rr}K_{r}G_{dd})^{-1}G_{dd} \right)^{-1} \left[ Y_{in} + G_{dd}(I + G_{de}G_{rr}G_{de}K_{r}G_{dd})^{-1}G_{dd} \right] \left[ (G_{de} - G_{di})G_{PLL}K_{r} - G_{de}G_{rr}G_{de}K_{r} + G_{PLL}^{*}K_{r} \right]$$

B. Input admittance with current and voltage control

To include the dc voltage controller to the transfer function matrix flow chart, voltage controller matrix $G_{cv}$ is introduced as shown in Fig. 11.

![Fig. 11. Transfer function matrix flow chart representation of VSC small signal model including PLL and current and voltage feedback control](image)

Fig. 12 shows the comparison between the simulation results (red curve) and analytical expression results (dotted blue curve), they are matching each other.

![Fig. 12. Verification of VSC input admittance including PLL and current voltage feedback control](image)

![Fig. 13. Comparison of VSC input admittance with different PLL bandwidth and current and voltage feedback control](image)

Fig. 13. Comparison of VSC input admittance with different PLL bandwidth and current and voltage feedback control
Fig. 13 shows the effect of the PLL and current plus voltage feedback control on the VSC input admittance. After close the voltage feedback control loop, VSC becomes a constant power load as shown in $Y_{dd}$ elements that phase of $Y_{dd}$ changes from 90° to 180° within the voltage control loop. Similar to the open loop and with current feedback control cases, PLL only affects the $Y_{dq}$ and $Y_{qq}$ elements, where a faster PLL will yield lower admittances within its bandwidth. Voltage feedback control loop can further lower the admittance compare with the one without voltage control.

IV. IMPACT TO SYSTEM STABILITY DUE TO PLL EFFECTS

The analysis shown in previous sections indicates that different PLL dynamics can change the input admittance of VSC, specifically, PLL will only change $Y_{dq}$ and $Y_{qq}$ elements of the admittance, faster PLL will give lower admittance within its bandwidth. Usually, VSC acts as load converter in a power conversion system, such as motor drive front end, it behaves as a constant power load. Under certain source impedance, unstable condition may happen. [3] shows the possibility that changes in the load converter admittance can cause instability in VSI feeding VSC system. This paper also explores that whether changing of PLL dynamics can cause instability in the system. The same setup as shown in [3] is used to demonstrate the instability caused by changing PLL bandwidth. System circuit diagram and the control scheme of are shown in Fig. 14. System parameters and VSI control parameters are shown in Table IV and Table V. VSC controller is the same as shown before. Two PLL with different bandwidth are used for demonstration. The first PLL design sets the bandwidth to be 1Hz the filter transfer function is shown in (21). The second PLL design sets the bandwidth to be 8Hz, and the filter transfer function is (22).

Switching model simulations are done using the parameters discussed before.

### TABLE IV. PARAMETERS OF THE SYSTEM

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
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<tbody>
<tr>
<td>$V_{dc,VSI}$ (V)</td>
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<td></td>
</tr>
<tr>
<td>$V_{dc,VSC}$ (V)</td>
<td>270</td>
<td></td>
</tr>
<tr>
<td>$f$ (Hz)</td>
<td>400</td>
<td></td>
</tr>
<tr>
<td>$C_{dc,VSI}$ (µF)</td>
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<td></td>
</tr>
<tr>
<td>$R_{LVSI}$ (mΩ)</td>
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</tr>
<tr>
<td>$L_{LVSI}$ (µH)</td>
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<td></td>
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<td>$R_{LVSC}$ (mΩ)</td>
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<tr>
<td>$L_{LVSC}$ (µH)</td>
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<tr>
<td>$R_{dc}$ (Ω)</td>
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<tr>
<td>$f_{s}$ (kHz)</td>
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### TABLE V. PARAMETERS OF VSI CONTROLLER

<table>
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<tr>
<td>$K_{ii}$</td>
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<td>$K_{pv}$</td>
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<tr>
<td>$K_{iv}$</td>
<td>41.879</td>
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</tbody>
</table>

$$f_{PLL_{1st}} = \frac{0.08921s + 3964}{s}$$   \hspace{0.5cm} (21)

$$f_{PLL_{2nd}} = \frac{0.7137s + 25.37}{s}$$   \hspace{0.5cm} (22)

Fig. 14. VSI feed VSC system diagram
Average simulation results of VSI output impedance and VSC input admittance with different PLL design are shown in Fig. 15. Although the PLL bandwidth is low, the same variation pattern for VSC input admittance as analyzed before can be observed.

![Fig. 15. Comparison of VSI output impedance and VSC input admittance with different PLL bandwidth](image)

Switching model simulation is first done for VSC with 1Hz PLL bandwidth. Fig. 16 shows the simulation results of PLL output frequency error respect to line frequency. At 1.2s, VSC feedback control starts. The system is stable as indicated by ac interface voltage and VSC dc voltage as shown in Fig. 17 and Fig. 18.

![Fig. 16. PLL output frequency error respect to line frequency for PLL bandwidth 1Hz](image)

Using output impedance of VSI and input admittance of VSC, GNC can be applied to the system. The characteristic loci shown in Fig. 19 indicates the system is stable. This means the system stability condition can be predicted by using source and load impedance.

![Fig. 19. Characteristic loci of stable case](image)

The simulation results for VSC with 8Hz PLL bandwidth is shown in Fig. 20 for the PLL output frequency error respect to 400Hz line frequency. VSC feedback control is still started at 1.2s. After the control starts, PLL output frequency begin to oscillate. Fig. 21 and Fig. 22 are the ac interface voltage and VSC dc output voltage. Both of them show that the system is in unstable condition. Using the corresponding impedance and admittance, GNC also shows the system is unstable.

![Fig. 20. PLL output frequency error respect to line frequency for PLL bandwidth 8Hz](image)
This paper studies the impact of the PLL on the input admittance of three-phase VSC. The analysis shows that PLL introduces parallel admittance to the open loop admittance of VSC. This parallel admittance only has value on its $dq$ and $qq$ elements and trying to lower the admittance with in the PLL bandwidth. Current and voltage feedback control have additional shaping effects on the admittance of VSC but the conclusion of PLL effect still holds. This paper also demonstrates the possible instability caused by different PLL design, GNC is applied to both stable and unstable cases, and system stability conditions can be predicted.

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