INFLUENCE OF ARC CAPPING LAYER ON STRESS INDUCED VOIDING IN NARROW ALCu METALLISATIONS

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Abstract: The influence of capping layer composition was examined in accelerated stress-migration performance of AlCu(0.5%) narrow stripe lines. Using resistance monitoring and Scanning Electron Microscopy, we determined that metallisation with bilayer Ti/TiN ARC top layer induced more stress voiding than metallisation with single TiN ARC layer. These experimental results are discussed on the basis of a void growth mechanism provided by diffusion at the interface between AlCu and ARC top layer.

INTRODUCTION

Electromigration and stress-migration in metallisations are major reliability issues for interconnection lines of advanced ICs. It is generally considered that voiding mechanisms are reduced for improved line microstructure: large grain size and high (111) oriented texture [1] but is enlarged in narrow lines [2]. More generally, stress voiding is the consequence of the relaxation of thermal stress provided by cooling the metallisation after high temperature process (450 °C). Stress relaxation rate is high between 150°C and 250°C where the combination of stress driving force and mass transport is maximised [3].

In the present study we propose an analysis of stress voiding in AlCu(0.5%) interconnections of 0.25 μm CMOS technology [4] after annealing at 200°C & 250°C during 1800 h. The results obtained are compared, versus the composition of ARC top layer: TiN or Ti/TiN; the addition of Ti, in ARC layer may help electromigration resistance when Al₃Ti precipitates reduce interfacial diffusion [5].

SAMPLE CHARACTERISTICS

A Ti/TiN barrier layer was DC sputtered at 350°C on a Si substrate covered with PECVD SiO₂, then AlCu metallisations were DC sputtered at 450°C. ARC layers were in situ deposited at 350°C and, on top, a HDP SiO₂ passivation layer was deposited. The cross section of the metallisation is shown in the figure 1.

Figure 1: Cross-section of the test structure
The thickness of the metal structures investigated are, from Si substrate to top:
a) SiO$_2$(600nm)/Ti(40nm)/TiN(60nm)/AlCu(0.5\%)440nm/TiN(40nm)/SiO$_2$(700nm)
b) SiO$_2$(600nm)/Ti(40nm)/TiN(60nm)/AlCu(0.5\%)440nm/Ti(10nm)/TiN(40nm)/SiO$_2$(700nm).

Microstructure characterisation was performed on full sheet wafers. For both metallisations, average grain size ($d$), measured from AFM observations and texture, characterised with the full width at half maximum value of the (111) rocking curve ($\omega$) using X ray diffraction, have the same values (see table 1).

Stress change of the AlCu metal structures during thermal cycle was determined with wafer curvature measurements and is shown in the figure 2.

At room temperature, after a backend anneal at 425 $^\circ$C for $\frac{1}{2}$ h, the stress level of full sheet metal was 100 MPa for both structures, which is a usual value for Al.

Then increasing temperature provided a linear decrease of the stress level following an elastic regime described by equation (1). At 250$^\circ$C plastic deformation occurred leading to final stress levels that are higher than the initial values.

In the elastic regime, the same stress level is measured in both samples. In narrow lines, cooling from the high temperature process provides in metal elastic stress which can be expressed as follow:

$$\sigma_{Al} = \frac{E_{Al}}{1 - \nu_{Al}} \times \Delta \alpha \times \Delta T$$

where $E_{Al}$ are the Young modulus and $\nu_{Al}$ the Poisson ratio of Al, $\Delta \alpha$ the difference in thermal expansion coefficient between Al and Si, and $\Delta T$ the difference of temperatures between the high temperature of process and the actual temperature of experiences. So during the annealing, the same stress level is expected for both metal structures.

**RESISTANCE VARIATION**

Stress-migration experiments consisted in aging at room temperature, at 200$^\circ$C and 250$^\circ$C, in air, long meander lines: length = 0.454m and width = 0.4 $\mu$m. Resistance measurements were performed at room temperature before aging began ($R_0$) and also at periodic intervals during aging up to 1800 h. A population of 13 lines was used for each experimental condition. Figures 3 & 4 show the average value of relative resistance change $\Delta R/R_0$ versus aging time. Since every line has a similar behavior, an average value is presented for clarity. For both sample structures, a decrease of resistance is observed during the first 100 h aging at 200$^\circ$C and 250$^\circ$C. This phenomenon is due to Al$_2$Cu precipitation [6] because Cu is in solid solution in Al after the backend anneal at 425$^\circ$C for 30 minutes.
For metal structure with TiN ARC little variation of resistance is observed for longer time and both aging temperatures. On the contrary, metal structure with Ti/TiN ARC gives rise to a significant amount of resistance increase after 1800 h at 200°C or 600 h at 250°C. For a second time step at 250°C, an additional resistance decrease is observed, not yet understood. It is to be noticed that resistivity evolution during aging of these metal structures does not exhibit any further variation after an initial decrease, thus indicating that the resistance variation encountered in narrow lines is probably due to voiding. For comparison, resistance of samples held at room temperature was monitored with the same procedure.

VOID GROWTH MODEL

The magnitude of the resistance shift produced in a line of initial length $L_0$, by a void length, $L_v$, extending through the whole metal line width and thickness, and leaving the refractory layer as the only conductive path can be expressed as follows:

$$\Delta R = \frac{L_v \times \rho_R \times t_A}{R_0} \frac{L_0 \times \rho_A \times t_R}$$

with $\rho_A$ and $t_A$ the resistivity and thickness of the metal line, $\rho_R$ and $t_R$ the parameters of the refractory layer and $\rho_A << \rho_R$ and $t_R << t_A$.

If void growth occurs due to a diffusion process as proposed by [7], the cumulated void length, $L_v$, can be expressed versus time $t$, using a diffusion coefficient $D$:

$$L_v = \frac{12 \times \Delta \alpha \times \Delta T}{\sqrt{\pi}} \times N_v \times \sqrt{D \times t}$$

with $N_v$, the number of voids in the stripe line.

Thus fractional resistance increase follows a $\sqrt{t}$ law as experimentally observed in figure 4. According to the previous equations, the amount of resistance shift should also decrease when aging temperature increases up to the process temperature as observed (see table 1).

SEM observations of void morphology after 1800 h aging at 200°C are shown in figures 6 & 7 for both structures. As expected from the measurements of resistance shift, many large voids severing the Al/Cu line test are observed. Void length up to 1µm is measured in metal
structure b). Fewer and smaller voids are observed in metal structure a), thus inducing a smaller resistance increase.

The occurrence of diffusion at the interface between AlCu and its ARC layer has also be experimentally measured in similar metal structures subjected to electromigration experiments [8].

**Table 1:** Microstructure and stress-migration typical parameters of metal structures

<table>
<thead>
<tr>
<th>Metal structure</th>
<th>d (μm)</th>
<th>ω (°)</th>
<th>ΔR / Ro</th>
<th>Lυ (μm)</th>
<th>Nυ(μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARC = TiN @ 200°C</td>
<td>2.6</td>
<td>7.5</td>
<td>0.010</td>
<td>22.5</td>
<td>6.2 10⁻³</td>
</tr>
<tr>
<td>@ 250°C</td>
<td></td>
<td></td>
<td>0.004</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>ARC = Ti/TiN @ 200°C</td>
<td>2.5</td>
<td>6.9</td>
<td>0.044</td>
<td>100</td>
<td>13 10⁻³</td>
</tr>
<tr>
<td>@ 250°C</td>
<td></td>
<td></td>
<td>0.020</td>
<td>45</td>
<td></td>
</tr>
</tbody>
</table>

**CONCLUSION**

In AlCu(0.5%) metallisation for 0.25 μm CMOS technology, stress relaxation of narrow lines (0.4 μm) accelerated at 200°C provided large voids, up to 1 μm, which extend through the whole line width and thickness. The experimental results are consistent with a void growth mechanism by diffusion. The comparison of lines which offers the same microstructure and stress level but have Ti/TiN or TiN capping layer shows that on one hand interfacial diffusion is not suppressed by the 10 nm Ti layer added on top of the AlCu and on the other hand, the number of voids is increased.

**References**
