Design of FC-AE-1553 interface GPS module

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Abstract—Based on the analyzing of FC-AE-1553 protocol, this paper has completed a design of FC-AE-1553 interface GPS module by taking FPGA as the core controller and building Qsys system on chip. As a sensor Network Terminal (NT) in FC-AE-1553 network, the module shall give a correct response to a Network Controller (NC). It also transmits data received from GPS receiver to a FC-AE-1553 network by FC-AE-1553 interface. Finally, a test platform based on Fibre Channel network is build to verify the design.

Keywords - FC-AE-1553, GPS receiver, Network Terminal.

I. INTRODUCTION

With the advantage in data rate and network performance\(^1\), FC-AE-1553 based on Fibre Channel technology may probably be the new generation of military bus standard following MIL-STD-1553B\(^2\), and there will be more and more its applications in spaceborne and airborne systems\(^3\)[4]. So the research on FC-AE-1553 protocol and the development on standard instruments are of great significance for realizing the overall upgrading of avionics system.

Via the analyzing of FC-AE-1553 protocol, a design method is proposed to GPS Module with FC-AE-1553 interface. The module can receive information including time, latitude, and longitude from satellites via GPS receiver, and transmit data received from GPS receiver to a FC-AE-1553 network via standard FC-AE-1553 interface in order to timing the network. In addition, as a Network Terminal (NT) in network, it shall give a correct response to Network Controller (NC) commands\(^5\)[6].

II. SCHEME DESIGN

FC-AE-1553 interface GPS Module consists of standard FC-AE-1553 interface, processor, standard RS232 interface and GPS receiver. Figure 1 presents the design scheme of the module.

- FC-AE-1553 Interface
- Processor
- RS232 Interface
- GPS Receiver
- Antenna
- FC-AE-1553 Network

Figure 1. Design Scheme of the Module

FC-AE-1553 interface can transmit high speed data with standard format specified in the underlying protocol of Fibre Channel. FC-AE-1553 interface consists of interface circuit and interface logic. Optical transceiver is used to complete photoelectric conversion in the interface circuit. Interface logic, which is programmed in FPGA, calls transceiver hard core embedded in FPGA to complete deserialization. In this way, the high speed serial signal on bus is converted to low speed parallel signal, which is convenient for the following circuit design. Then, sending module, receiving module and port state machine module are programmed as a part of the interface logic. The three parts work together to complete variety functions such as 8b/10b encoding and decoding, frame transceiver, flow control.

The M12MT receiver is selected as GPS receiver, which output follows the Motorola binary standard. The output begins with “@@” (4040H) and ends with “\(\text{<CR><LF>}\)” (0daH), including time, latitude, longitude, altitude and other valid information between them. The receiver send received data via RS232 bus, so RS232 interface shall be implemented in FPGA in order to communicate with GPS receiver.

Processor, which manages the module, can read data from the interfaces and make analysis to get valid information. It can also write encapsulated standard data into the interfaces to send. Interface functions are realized by programming in FPGA, so we select NIOS II soft core processor embedded in FPGA as the processor. Compared with ARM, PowerPC processor, it communicates with the interfaces easier. This greatly simplifies the design complexity.

III. QSYS SYSTEM DESIGN

As the design scheme above, embedded NIOS II in FPGA is selected as the processor. So Qsys system is build in FPGA to implement the scheme. Figure 2 presents the structure of Qsys system.

Fibre interface module, encapsulated according to the Qsys system demand, is the interface logic of FC-AE-1553 interface. On the one hand, it caches the received data and then informs NIOS II to read. On the other hand, it sends the data written by NIOS II. Similarly, RS232 interface module caches data transmitted by GPS receiver and then waits NIOS II to read. Both communicate with NIOS II using Avalon local bus.
JATG-UART module is the interface to debug Qsys system via JATG cable. Program in NIOS II can be debugged on computer via the module. EPCS controller module is the interface to control EPCS4, from which FPGA loads configuration information each time the system powers up. DDR II controller module is the interface to control DDR SDRAM to store data.

When FC-AE-1553 interface receives data, NIOS II will read it in time and then judge whether it is a command frame or not. If the answer is positive, NIOS II will analysis the command frame to extract the SEQ_ID and the number of frames. Then it confirms the transmission is either write-type commands or read-type commands. In read-type commands, NIOS II will receive data frames from NC and store them into DDR SDRAM. When the receiving is completed, whether to send a status frame depends on the value of suppress status.

In write-type commands, data frames containing GPS valid information are needed to send to NC. NIOS II will firstly read data received by GPS receiver from RS232 interface and extract 152 bytes of valid data. Then it inserts this data into FC-AE-1553 standard data frame. Finally, this encapsulated data frames will be transmitted to FC-AE-1553 interface to send. Figure 4 shows the encapsulated data frame format.

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Figure 2. Structure of the Qsys System

IV. SOFTWARE DESIGN

The software design is C language programming in NIOS II for data analysis and transmission control. FC-AE-1553 is based on command response type. As a NT in the network, the module shall analysis command frame after receiving a command frame and then give responses according to the result of analysis. The analytic content includes either sending or receiving, whether to suppress status or not, etc. Specific software design flowchart is shown in figure 3.

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<table>
<thead>
<tr>
<th>SOF 4bytes</th>
<th>Frame Header 24bytes</th>
<th>GPS Valid Data 152bytes</th>
<th>CRC 4bytes</th>
<th>EOF 4bytes</th>
</tr>
</thead>
</table>

Figure 3. Software Design Flowchart

V. VERIFICATION

A. Test Platform based on Fibre Channel Network

A test platform based on Fibre Channel network is build to test basic functions of the module, which consists of NC card, personal computer, Fibre switch and FC-AE-1553 interface GPS module (NT). Figure 5 shows the connection in test platform.

Figure 4. the Encapsulated Data Frame Format

Figure 5. the Connection in Test Platform

NC card can implement NC basic functions specified in FC-AE-1553 protocol, and the computer responses for controlling the NC card to send command frame and data frame via PCIe bus, and displaying the status frame and data frame received by NC.

Fibre switch is the Qlogic Company sanbox5600 switch used in SAN network. Although the switch is designed for SAN network, it supports FC-SW-2 protocol and be used for Fibre Channel Network after correctly setting. The switch includes 16 ports with data rate up to 4Gbps and supports assigning the network address.

B. Functional Test of the Module

Functional Test of the Module is the write-type commands (NC to NT transfers) test. For the design module, the write-type commands is sending received GPS data to NC. The computer control NC to implement the write-type commands transfers and display the GPS valid data received by NC.
Figure 6 shows the GPS valid data received by NC. We can get time information from it through analysis. 0607h represents June 7, 07DCh represents 2012, 10292Eh represents 16:41:46 and 00065D10h represents the decimal part of second. Combination of them is June 7, 2012 16:41:46.417040, which is the same as local time.

![Figure 6. GPS Valid Data Received by NC](image)

The analytic result illustrates normal communication between NC card and the module. Through further analysis, we can find out that the FC-AE-1553 interface conforms to standard specification and NIOS II and GPS receiver both work properly. Therefore, the design having been verified is rational and feasible.

VI. CONCLUSION

With research on the new generation of avionics system bus, this paper carries out the design of FC-AE-1553 interface GPS module. The design is completed by the scheme of standard interfaces programmed in FPGA and embedded processor central control. A test platform based on Fibre Channel network is build to test the NC to NT transfers of the module. The result illustrates normal communication between NC card and the module. The design having been verified is has guiding significance to NT development.

REFERENCES


