Reliability improvement in GaN HEMT power device using a field plate approach

Wen-Hao Wu, Yueh-Chin Lin, Ping-Chieh Chin, Chia-Chieh Hsu, Jin-Hwa Lee, Shih-Chien Liu, Jer-shen Ma, Hiroshi Iwai, Edward Yi Chang, Heng-Tung Hsu

Abstract

This study investigates the effect of implementing a field plate on a GaN high-electron-mobility transistor (HEMT) to improve power device reliability. The results indicate that the field plate structure reduces the peak electrical field and interface traps in the device, resulting in higher breakdown voltage, lower leakage current, smaller current collapse, and better threshold voltage control. Furthermore, after high voltage stress, steady dynamic on-resistance and gate capacitance degradation improvement were observed for the device with the field plate. This demonstrates that GaN device reliability can be improved by using the field plate approach.

1. Introduction

Improving efficiency has become a crucial issue for power electronics. Silicon-based power devices have been widely used over the past several years, but their performance cannot meet future requirements of low power loss [1,2]. GaN offers a unique combination of properties such as a high breakdown field, high electron mobility, and high peak electron velocity [3–8]. GaN high-electron-mobility transistors (HEMTs) have been widely investigated, with reports of superior performance including high output power density (10 W/mm at 40 GHz) [9], a high cutoff frequency (fT) of 400 GHz [10], a high breakdown voltage of 1590 V, and a low specific on-resistance of 1.86 mΩ cm [2,11]. However, reliability is essential for future commercial applications. High performance without degradation under long-term high voltage operation is a key issue for GaN-based devices in power electronics applications. Degradation through the inverse piezoelectric effect has been observed in GaN HEMTs. It considerably affects device reliability, and must be overcome for high power applications of GaN HEMTs to be feasible. Many solutions have been proposed, such as chemical surface treatments and passivation materials [12,13]. T-gate structures have also been implemented in GaN HEMTs to improve device performance and reliability [14]. Because the gate capacitance degradation caused by defect generation after a device is biased at high voltage, results in device threshold voltage (VTH) shift [15] and current collapse, as a result, stability of device gate capacitances can be used to reflect device reliability. Field plate technology has been widely used to enhance device breakdown [16] and suppress current collapse [17]. However, the use of field plate to eliminate gate capacitance degradation for device reliability improvements has not been fully explored. In this study, GaN HEMT devices with field plates (FP-GaN HEMT) were fabricated and the effects on electrical performance, gate capacitance and reliability were investigated.

2. Device fabrication

The Al0.22Ga0.78N/GaN HEMTs structure was grown on a 6-inch Si substrate using metalorganic chemical vapor deposition (MOCVD) technology. The layer structure from bottom to top includes a 1 μm GaN buffer layer, a 20 nm AlGaN barrier layer, and a 3 nm GaN cap layer. The device fabrication process includes the following steps: Ohmic contact formation, mesa isolation, gate...
formation, passivation, and field plate formation. A Ti(20 nm)/Al (120 nm)/Ni(25 nm)/Au(100 nm) metal structure was deposited as Ohmic metal by an E-gun evaporator and thermally alloyed at 800 °C for 1 min by rapid thermal annealing to form the Ohmic contacts. The device source-drain spacing in this study was 20 μm. The device’s active region was defined by mesa etching using an inductively coupled plasma machine with a 200 nm etching depth. A Ni(50 nm)/Au(200 nm) film was deposited as the gate metal with a 2 μm gate length. Subsequently, a 200 nm SiNx film was deposited as the passivation layer by plasma-enhanced chemical vapor deposition. Finally, SiNx in the gate pad area was etched and Ni(50 nm)/Au(200 nm) metal was deposited as field plate metal, which was connected to the gate pad to form the HEMT with the field plate. For performance comparison, a GaN HEMT without the field plate (NFP-HEMT) was also fabricated. Cross sections of the NFP-HEMT and FP-HEMT devices are shown in Fig. 1 (a) and (b), respectively.

3. Results and discussion

Fig. 2 compares the DC characteristics of NFP-HEMT and FP-HEMT. The FP-HEMT has a lower steady-state drain-source current (I_DSS) of 345 mA/mm at V_DS = 20 V (NFP-HEMT I_DSS: 375 mA/mm), and similar maximum drain-source currents (I_DSmax) were observed (630 mA/mm for FP-HEMT and 628 mA/mm for NFP-HEMT) when biased at V_GS = 2 V. The V_TH shifted from −3.9 V to −3.5 V when using the gate field plate. The large V_TH shift was obtained because of a smoother electric field distribution, which was achieved for both the vertical and horizontal electric fields [18] by using the gate field plate. Furthermore, the high vertical electric field at the drain edge of the gate was reduced due to the gate field plate, which effectively decreased the inverse piezoelectric effect and eliminated the trapped electrons at the AlGaN surface [19–21]. The FP-HEMT in this study also shows a higher maximum extrinsic transconductance (G_mmax) of 138 mS/mm as compared to the data of G_mmax (135 mS/mm) for NFP-HEMT. The slightly higher G_mmax value for the FP-HEMT is due to the trapped electrons at the AlGaN surface were released, hence enhancing the gate controllability. Fig. 3 shows the off-state leakage currents of the FP-HEMT and NFP-HEMT. The I_DS was extracted at V_GS = −5 V and the breakdown voltage was defined at a leakage current of 1 mA/mm.

Fig. 3(a) indicates that the device breakdown voltage was improved from 335 V to 365 V by using the field plate. Furthermore, the gate leakage of the FP-HEMT was almost 10 times smaller than that of the NFP-HEMT because of the smooth electric field distribution caused by the gate field plate, which also effectively reduces the inverse piezoelectric and electron tapping effects in the AlGaN barrier layer. The leakage current reduction could be because of the reduction of defect-formation in the leakage path between the gate and the channel. In summary, the V_TH shift to positive and the G_mmax increase were caused by improved gate control ability in the device with the field plate. Furthermore, the breakdown voltage increased because of the smooth electric field distribution after the field plate was implemented. Table 1 compares the DC characteristics of FP-HEMT and NFP-HEMT.

The performances of the FP-HEMT and the FNP-HEMT were evaluated at off-state status with V_DS = 100 V and V_GS = −5 V. In general, the current decreased during the high voltage stress and recovered after the stress was terminated. Two mechanisms account for the current degradation: charge injection into the surface, and defect generation [7]. Charge injection causes the tempo-
rary reduction of the drain current that occurs when electrons remain trapped at the surface after a large bias is applied to the drain, and over 90% can be recovered in 1 min \[22\]. However, defect generation is irreversible, being caused by the inverse piezoelectric effect in the AlGaN barrier layer. Therefore, we measured the IDS-VGS curve after 1 h high voltage stress, and maintained floating for 10 min to relax most of the electron trapping effect. Fig. 4(a) and (b) show the IDS versus VGS curves for the FP-HEMT and FNP-HEMTs devices respectively, before high voltage stress, at 1 h and 2 h of stress, and at 10 min recovery after the 2 h of stress was terminated. The IDSmax of the NFP-HEMT decayed to 74% after 1 h of stress and 48% after 2 h. The current of the 2 h stressed device recovered to 54% after the high voltage stress was terminated for 10 min. However, the IDSmax degradations of the FP-HEMT were decayed to just 91% after 1 h and 80% after 2 h, and recovered to 85% after the stress was terminated for 10 min. This suggests that a field plate can effectively reduce the inverse piezoelectric effect, resulting in lower electric field crowding in the drain side of the gate edge and successfully reducing the tensile strain in the AlGaN barrier layer.

Fig. 5(a) and (b) shows the IDS versus VGS curves with VGS bias from 2 V to \( \frac{-5}{C_0} \) V and then from VGS of \( \frac{-5}{C_0} \) V to 2 V for NFP-HEMT and FP-HEMT, before and after 2 h of stress. Neither device showed a hysteresis effect before stress. However, the NFP-HEMT suffered severe hysteresis in the IDS-VGS loop measurement after high voltage stress, indicating that FP-HEMT has less electron trapping at the interface than NFP-HEMT. Fig. 6 compares the dynamic Ron change for FP-HEMT and NFP-HEMT after 2 h of high voltage stress. For the dynamic Ron measurement, first the device was turned OFF for 10–120 min at 100 V stress voltage, and then the device was turned ON with a switching time of 0.1 s for IDS-VDS measurement. The dynamic Ron (\( R_{\text{in}} = \frac{dV_{\text{DS}}}{dI_{\text{DS}}} \)) of the NFP-HEMT increased drastically after 20 min, and continued increasing even after 110 min. However, for the FP-HEMT, the dynamic Ron increased slightly in 10 min, and then remained constant after 2 h of stress, as indicated in Table 1. It is evident that the HEMT with the gate

<table>
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<td>Comparison of the DC characteristics for NFP-HEMT and FP-HEMT after 1 h and 2 h stress and 2 h stress with 10 min. recovery with stressed at VDS = 100 V and VGS = ( \frac{-5}{C_0} ) V.</td>
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<tr>
<td>Off-state IDS (mA/mm)</td>
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<td>FP-HEMT</td>
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<td>NFP-HEMT</td>
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field plate can suppress the electron trapping effect and reduce current collapse [16,23] during long-term high voltage stress.

To investigate the surface trapping effect, the pulse IDS-VDS curve was measured with a pulse width of 45 ms (Fig. 7). The NFP-HEMT I-V curves show only a slight difference between the pulse and DC measurements before the stress [Fig. 7(a)]. However, a severe degradation in the pulsed measurement after stress testing for 2 h was observed. This was caused by defect generation and an interface trap increase, and eventually led to the current degradation and obvious decay of on-resistance (Ron) for the device. Fig. 7(b) shows the pulsed IDS-VDS for the FP-HEMT before and after stress. The pulsed and DC I-V curves show almost the same value, indicating that the field plate structure can effectively suppress the trapping effect compared to the NFP-HEMT.

The S-parameters of the FP and NFP devices were measured from 100 MHz to 4 GHz using an Anritsu 37369 C vector network analyzer at VDS = 10 V and IDS = 0.5 IDSS. A small-signal model was built for the two devices, and the parasitic capacitances including gate-source capacitance (CGS) and gate-drain capacitance (CGD) for NFP-HEMT and FP-HEMT were extracted to study the capacitance change caused by the defect generation. Table 2 lists the capacitances before and after stress, showing that the CGS and CGD of the NFP-HEMT increased drastically (about 51% and 218%, respectively) after 2 h of high voltage stress at 100 MHz. This degradation is because of the defect generation at the drain side of the gate edge [24]. However, the capacitance increase in FP-HEMT (CGS increased 4%, and CGD 32%) is small compared to that of NFP-HEMT (CGS 51%, CGD 218%). This demonstrates that HEMT with a gate field plate structure can effectively suppress the electron tapping effect as a result of less defect generation caused by alleviating the piezoelectric effect. Furthermore, the CGD increase is higher than that of CGS after stress because of higher electric field crowding in the drain side of the gate edge.

4. Conclusion

In summary, the field plate structure reduces the peak electrical field strength and thus reduces the interface traps in the GaN
HEMT, resulting in higher device breakdown voltage, less gate leakage current, and improved threshold voltage control. The stability of the dynamic on-resistance and the gate capacitance degradation after high voltage stress were improved due to the suppression of the defect generation in the FP-HEMT. Furthermore, the increase of CGD is higher than that of CGS after the stress because of higher electric field crowding in the drain side of the gate edge. Thus, the adoption of the field plate structure in the GaN HEMT can improve both the performance and reliability of the device under high voltage stress.

Acknowledgment

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Table 2
Comparison of the intrinsic capacitances for NFP-HEMT and FP-HEMT before and after stress at Off-state condition with \( V_{DS} = 100 \, \text{V} \) and \( V_{GS} = -5 \, \text{V} \) for 2 h.

<table>
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<th>Capacitance before stress</th>
<th>Capacitance after 2 h stress</th>
<th>Capacitance change AC</th>
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<tr>
<td></td>
<td>CGS (nF/mm)</td>
<td>CGS (nF/mm)</td>
</tr>
<tr>
<td>FP-HEMT</td>
<td>1.27</td>
<td>13.50</td>
</tr>
<tr>
<td>NFP-HEMT</td>
<td>0.59</td>
<td>11.40</td>
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The italic values are to highlight the incremental change as compared to the nominal values.

References


Fig. 7. Comparison of Pulse and DC IDS versus \( V_{GS} \) for the devices before and after stress at Off-state with \( V_{GS} = 100 \, \text{V} \) and \( V_{GS} = -5 \, \text{V} \) for 2 h: (a) NFP-HEMT, and (b) FP-HEMT.
Dr. Hsu received his B.S. and M.S. in electronics engineering from National Chiao Tung University, Taiwan in 1993 and 1995, respectively, and his Ph.D. degree in electrical and computer engineering from University of Maryland, College Park, in 2002. From 1997 to 2005, he served as the Director of Engineering of AMCOM Communications, Inc., Gaithersburg, MD. From 2006 to 2015, he was with the Department of Communication Engineering in Yuan Ze University. Since 2015, he joined the International College of Semiconductor Technology, National Chiao Tung University (NCTU), where he is currently an Associate Professor. His research interests in recent years include the design and implementation of RF front-ends, millimeter wave circuits, high-frequency packaging, and antenna designs. He has authored or co-authored more than 60 journal papers and held 3 U.S. patents. He was also a recipient of the 2012 Y. Z. Hsu’s Outstanding Professor Award.
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