A 255nW 138kHz RC Oscillator for Ultra-low Power Applications

Yao Wang*, Liang Rong, Liangbo Xie, Jiaxin Liu, Guangjun Wen

School of Communication and Information Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China
* Email: wangyao@uestc.edu.cn

Abstract
An on-chip sub-µW RC oscillator suitable for ultra-low power applications is presented. A technique that cancels both comparator delay and offset are proposed to improve the frequency stability against variations of temperature and supply voltage. This relaxation oscillator is designed and simulated in a 180-nm CMOS technology. The post layout simulation results show that the proposed circuit has a 1-cycle start-up time, and the frequency drift is less than ±0.6%. For the supply voltage changing from 0.9 to 1.2 V, the variation of frequency is −0.72% ~ +0.68% and the temperature coefficient is 75.5 ppm/°C over 0 to 90°C. The power consumption of the proposed oscillator is 255 nW at TT and 27°C.

1. Introduction
Recently, nano-power on-chip reference oscillators are required for ultra-low power one-chip applications including wireless sensor nodes, implantable chips and radio frequency identification (RFID) transponders. The frequency stability of the oscillator against temperature and supply variations is a critical specification for an on-chip oscillator. However, aggressive reduction of the power consumption significantly increases the circuit performance variation, and constrains the use of complex digital calibration methods. Compared to energy-hungry LC oscillators, RC oscillators have been considered to be more suitable for low-power applications due to the simple structure, low power consumption and relatively high accuracy after trimming.

Figure 1(a) presents the block diagram of a conventional RC oscillator. Ideally, the voltage $V_C$ rises while charging by $I_{B1}$. If $V_C > V_{H}$, a comparator sets RS flip-flop and changes the state of oscillator into discharging phase; then $V_C$ falls while discharging by $I_{B2}$. If $V_C < V_{L}$, another comparator resets RS flip-flop and the state returns to charging phase. The output clock frequency is mainly determined by the value of RC and the performance of comparators including the delay $t_d$ and the offset $V_{OS}$. Variations of comparator’s delay $t_d$ and offset $V_{OS}$ result in frequency variation with voltage and temperature. In particular, when the bias current of the comparator is reduced for nano-power consumption, $t_d$ and $V_{OS}$ are increased and not neglectable for high frequency oscillators. While variations in $R$ and $C$ with respect to process, temperature and supply voltage variations can be kept low through trimming and the use of appropriate devices, the oscillators suffer from $t_d$ and $V_{OS}$ variations.

To solve these issues, a number of low power RC oscillator circuits have been reported and different techniques to improve the output clock stability with reduced power supply have been presented in the past few years. A Feed forward Period Control Scheme is reported in [1]. A replica oscillator is utilized to measure $t_d$. The core oscillator employs a bi-state current-source for boost and normal charging, so as to charge the capacitor with 2X charging current during a period equal to $t_d$. This technique minimize the effect of comparator delay, but can not address the frequency variation due to comparator offset. Another work presents a comparator offset cancellation method for RC oscillator[2]. However, it still suffers from frequency variation caused by comparator delay. Therefore, it is highly desirable to develop a RC oscillator that can cancel the effect of comparator delay and offset at the same time. In this paper, we propose an RC oscillator architecture that cancels both delay and offset of the comparators. This technique makes the output clock frequency only depends on the value of RC theoretically. Therefore, the proposed technique minimizes frequency variations with temperature and supply voltage, and looses the constraints on the design of comparator.

Figure 1 Conventional RC oscillator.

The rest of the paper is organized as follows. Section 2 describes the proposed RC oscillator as well as its design optimization issues. Section 3 presents the simulation results. The paper is concluded in Section 4.
2. Proposed RC oscillator

The proposed low power RC oscillator is shown in Figure 2. It consists of two sub-oscillators. For the convenience of discussion, we refer to the left sub-oscillator as CO (core oscillator) and the right sub-oscillator as AO (auxiliary oscillator). All the branches of AO and CO are biased with the same current $I$. CO employs a similar circuit architecture as reported in [2].

The voltage waveforms of some key nodes are shown in Figure 3. For the sake of simplicity, we neglect AO and the branches gated by M1 and M2, and focus on the CO at first. When $Q_1 = 0$, switches M3 and M5 are on while M4 and M6 are off. $V_1$ increases as current $I$ passes through M3 and charges $C_1$. Meanwhile, a current $I$ passes through M5 and generates a reference voltage $V_{ref}$ at node $V_2$. When $V_1$ is higher than $V_2$, the output of COMP1 and SR1 changes leading to the state transition of M3~M6, then $C_2$ is charged and $V_1$ is fixed as the reference voltage. Therefore, the comparator offset affects the two phases of the period in different directions as shown in Fig. 3. Without boost-charging and AO the period of CO can be expressed as

$$T_{aco} = 2RC + 2t_d$$  \hspace{1cm} (1)
frequency is cancelled precisely. We employ AO to measure $t_d$ and generate signals $S_1$ and $S_2$ to control the boost charging switches M1 and M2. COMP2 is a replica of COMP1, and the initial level of the COMP2 inputs ($V_3$ and $V_4$) are set to $V_{ref}$. Assuming the initial states of $Q_1$ and $Q_2$ are “LOW”, hence $S_1$ and $S_2$ are “LOW”. When $Q_1$ and $Q_1B$ toggle, $S_1$ is pulled to “HIGH”, then capacitor $C_3$ begins to be charged, while capacitor $C_4$ is discharged. The COMP2 input $V_4$ is clamped to $V_{ref}$, and $V_3$ is increased until the COMP2 output toggles, then $S_1$ falls to “LOW”. As the initial voltages of $V_3$ and $V_4$ are both clamped to $V_{ref}$, COMP2 operates immediately after the CO outputs toggling, hence the pulse-width of $S_1$ and $S_2$ is equal to $t_d$ approximately. The boost-charging currents controlled by $S_1$ and $S_2$ are turned on at the beginning of every half cycle period, and last a period of $t_d$ approximately. Therefore, the period of CO with boost-charging can be theoretically expressed as

$$T_{osc} = 2RC$$

(2)

Note that the effect of comparator delay and offset is cancelled, and the oscillation frequency is only determined by the resistor $R$ and the charging capacitor $C$. To improve the temperature coefficient of the proposed oscillator, the resistor $R$ is composed of two different types of resistors, which have opposite temperature coefficients.

3. Simulation results

The proposed oscillator is designed based on a 180 nm CMOS technology, and post-simulated with different process variations, supply voltages and temperatures. The post-layout simulations validate the frequency accuracy, the PVT stability of frequency and the total power consumption of the proposed scheme.

This design has very short start-up time and high frequency accuracy for the low power consumption applications. Figure 4 shows the transient simulation result about start-up sequence for the propose oscillator. The supply voltage is set to 1V and the temperature is set to 27°C at TT process corner. The oscillator starts to run at frequency 138 kHz after the oscillator enable signal reach high level. Meanwhile, the oscillation frequency becomes stable at the first period and the deviation is less than ±0.6%.

Figure 5(a) presents the oscillation frequency variation under different temperatures and three process corners. Over 0 to 90°C, the oscillation frequency variation is −0.33%~+0.35% at all corners. The temperature coefficient is 75.5 ppm/°C. Figure 5(b) shows a −0.72%~+0.68% frequency drift as the supply voltage changes from 0.9 to 1.2V at all corners.

Figure 6 shows the power consumption of the proposed oscillator. The typical power consumption is 255nW under TT and 27°C, and the maximum power consumption is 320nW at FF and 90°C.
To validate the proposed approach, a traditional RC oscillator without comparator delay and offset cancellation is also built up, and the simulation results of the traditional oscillator and the proposed design are summarized in Table 1. Both oscillators employ the same time constant $RC(R=1.25M, C=3pf)$. The center frequency of the proposed circuit is 138 kHz, which is close to the theoretical frequency 133 kHz. However, the center frequency of the traditional oscillator falls to 84 kHz due to comparator delay and offset. Furthermore, this design can improve the frequency stability 4X against temperature and supply voltage variations. Table 2 compares this work with previous works. This work offers advantages in terms of low power consumption, low variation with temperature and supply voltage and 1-cycle start-up time.

4. Conclusions

A nano-power, fast start-up and high accuracy RC oscillator for ultra-low power applications is designed and simulated in a 180nm CMOS technology. An comparator delay and offset cancellation scheme has been presented that helps achieve temperature stability of 75.5 ppm/°C. The oscillator offers a good balance between power and frequency stability, which are both critical specifications for ultra-low power applications.

Table 1. Summary of simulation result

<table>
<thead>
<tr>
<th>Property</th>
<th>Without delay and offset cancellation</th>
<th>With delay and offset cancellation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>84 kHz</td>
<td>138 kHz</td>
</tr>
<tr>
<td>Variation with Temp (0~90°C)</td>
<td>-3% ~ +0.1%</td>
<td>-0.33% ~ +0.35%</td>
</tr>
<tr>
<td>Variation with Voltage (0.9~1.2V)</td>
<td>-0.23% ~ +3%</td>
<td>-0.72% ~ +0.68%</td>
</tr>
</tbody>
</table>

Table 2. Performance comparison with previous works

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Process</th>
<th>Frequency</th>
<th>Start-up time</th>
<th>Variation with Temp.</th>
<th>Variation with Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>VLSI 12*</td>
<td>100 kHz</td>
<td>1cycle</td>
<td>±0.68% @-40 to 90°C</td>
<td>±0.82% @0.725 to 0.9V</td>
</tr>
<tr>
<td>[2]</td>
<td>65 nm</td>
<td>100 kHz</td>
<td>N/A</td>
<td>±1.1% @-20 to 80°C</td>
<td>±0.1% @1.12 to 1.39V</td>
</tr>
<tr>
<td>[3]</td>
<td>130 nm</td>
<td>1200 kHz</td>
<td>N/A</td>
<td>±0.25% @20 to 60°C</td>
<td>±0.4% @1.4 to 1.6V</td>
</tr>
<tr>
<td>[4]</td>
<td>180 nm</td>
<td>1.28 MHz</td>
<td>N/A</td>
<td>±0.7% @-20 to 80°C</td>
<td>±0.5% @0.8 to 1.1V</td>
</tr>
<tr>
<td>[5]</td>
<td>180 nm</td>
<td>138 kHz</td>
<td>1cycle</td>
<td>±0.33% @0 to 90°C</td>
<td>±0.72% ~ +0.68%</td>
</tr>
</tbody>
</table>

* Measurement results.
# Simulation results.

References


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