Design Consideration of a Static Memory Cell

KENJI ANAMI, MASAHIKO YOSHIMOTO, HIROFUMI SHINOHARA, YOSHIHIRO HIRATA, AND TAKAO NAKANO

Abstract—This paper describes design criteria for high-density low-power static RAM cells with a four-transistor two-resistor configuration. The states of the cell latch are expressed by a dc stability factor introduced from transfer curves of the inverters in the cell. The criteria feature using only static conditions for read/write/retain operations. The designed cell considering mask-misalignment measured $22.8 \times 27.6 \mu m$ with 2.5 $\mu m$ layout rules. From the evaluation of dynamic characteristics, it was shown that the 16K RAM using the cell had a sufficient operating margin.

I. INTRODUCTION

A MEMORY cell array occupies 50–70 percent of the total chip area in static MOS RAM's. Electrical characteristics of a static RAM depend strongly on the design of the memory cell. In order to obtain high-performance static RAM's, much has been done both in process technology and in design methods. Those in process technology include device scaling minimization [1] of the memory cell size, adopting high-impedance polysilicon resistors [2]–[5] as load elements in the cell, and double polysilicon technology [5].

The cell size of static MOS RAM's is determined by the minimum feature and the noise margin. The noise margin of the cell depends on the conductance ratio of the inverter transistor and the access transistor. The conductance ratio also partly determines the speed performance and the power dissipation of the RAM. Therefore, optimization of the memory cell in terms of device dimensions is important to obtain high-density static RAM's.

The conductance ratio has been selected about 1.5 to 5 in conventional designs [6]. By judicious memory cell design, it is possible to reduce the ratio without exceeding the stability margin.

Cell stability is influenced by the channel width mismatches or threshold mismatches in all paired devices. However, threshold mismatches caused by the nonuniformity of ion-implantation or gate-oxide thickness can be neglected as those transistors are placed adjacent.

The access transistor and bit line load transistor could be layed out so as not to be influenced by mask misalignment without chip area penalty. Thus, the channel width mismatches of these transistors can also be neglected.

In this paper, the channel width mismatches of inverter transistors are dealt with, including the threshold shift caused by the narrow width effect. A new dc stability factor of the latch was introduced to analyze quantitatively the memory cell operation.

Fig. 1. Schematic of the memory cell with the peripheral circuits.

II. CELL STABILITY

Memory cells with the peripheral circuits are illustrated in Fig. 1. The cell is the usual flip-flop circuit and consists of a pair of cross-coupled inverter transistors Q1 and Q2, two high-impedance polysilicon resistors R1 and R2 for the load elements, and a pair of access transistors Q3 and Q4 which are used as coupling devices for the read/write operation.

Since the memory cell is expressed as a closed-loop circuit made by two inverter stages, the states of the memory cell are analyzed by the corresponding two static voltage transfer curves shown in Fig. 2, where the output voltage of the inverter is plotted as a function of the input voltage. In this figure the existence of the cross points $A_1$ and $A_2$ indicates the bistable states and is the condition necessary for the nondestructive read operation and for data retention.

The area of the region surrounded by the two curves in Fig. 2 corresponds to the dc stability of the cell. A new stability factor is defined by the voltage margin $V_m$ between two curves as shown [7]. According to this conception, the voltage margins $V_{m1}$ and $V_{m2}$ shown in Fig. 2 are regarded as the factor that expresses the strength of the latch in the cell. When the two curves are asymmetrical about the line $\Gamma$, the lesser value of the voltage margins $V_{m1}$ or $V_{m2}$ is adopted as the factor of the stability.

Both voltage margins $V_{m1}$ and $V_{m2}$ are required to be positive in the read operation, and either the voltage margin $V_{m1}$ or $V_{m2}$ has to be negative in the write operation.

The stable read operation is incompatible with the quick write operation. To guarantee both the high-speed stable read operation and the sure write operation against the size mis-
matches of the pair transistors and various operating conditions, the memory cell has to be designed properly.

III. Design of the Memory Cell

1) Nondestructive Read Condition: The stored data of a memory cell selected by the word line and the column decoder has to be read nondestructively. That is to say, both the voltage margins \( V_{m1} \) and \( V_{m2} \) have to be positive. This limitation gives the maximum gate width of the access transistor.

In the read operation the actual load of the inverter consists of the resistors \( R1 \) and \( R2 \), the access transistors \( Q3 \) and \( Q4 \), bit line load transistors \( Q5 \) and \( Q6 \), input/output bus line loads \( Q7-Q10 \), and the transfer transistors \( Q11-Q14 \). The margin of the cell in the read operation is mainly determined by the size of the inverter transistors, the access transistors, and the load transistors of the bit lines. The margin especially depends on the channel conductance ratio \( G_D \) of the access transistor \( G_D \) and access transistor \( G_T \) since the impedance of the access transistor is larger than that of the bit line load. A relation between the voltage margin \( V_m \) and the channel width ratio \( W'/W_d \) of the access transistor and access transistor was simulated, including the short channel effects and narrow width effects of MOS transistors. The result is shown in Fig. 3. The figure indicates that the larger channel width ratio gives the larger margin in the read operation. It is noticed that the channel width mismatch reduces the voltage margin significantly.

2) Write Condition: In the static memory cell consisting of the flip-flop, the write operation is performed by forcing high and low voltage to a pair of bit lines. In a static MOS RAM, one bit line is kept to a precharged level, and the other is lowered to the level at which not only static write conditions are satisfied, but transient write conditions are also satisfied. \( V_{FL} \) is defined as the bit line voltage at which the data changes from a high state to a low state when the voltage of a bit line is lowered under static conditions. \( V_{FL} \) has to be set lower than that of a low readout level of a bit line. \( V_{FH} \) is similarly defined as the bit line voltage at which the data changes from a low state to a high state when the voltage of a bit line is raised under static conditions. In static MOS RAM's, the bit line of the unselected column is precharged to a high state. Therefore, \( V_{FH} \) has to be set to a higher level than the precharged level so as not to be miswritten. Since it is hard to change the memory cell state by applying a high voltage from a bit line, as a rule this condition is not serious.

The relation of a bit line level and the voltage margin \( V_m \) is shown in Fig. 4, where the parameter is the size mismatch of the inverter transistors. The bit line voltage at which the voltage margin \( V_m \) becomes zero corresponds to the level \( V_{FL} \). The asymmetrical memory cell caused by the size mismatch has two different \( V_{FL} \) levels, as shown in this figure since one state is easy to write (higher \( V_{FL} \)) and the other is hard to write (lower \( V_{FL} \)). The larger size mismatch results in a larger difference between the two \( V_{FL} \) levels.

3) Data Retention Condition: This is the condition that the memory cell is not disturbed by the bit line voltage set in the previous read cycle. At the previous read cycle one of the memory cells in a column is selected by a word line. As a result, the bit line is driven by the memory cell and one of a pair of the bit lines is set to a low voltage. Here, only the bit line load transistors \( Q5 \) and \( Q6 \) act as a pull-up device. Input/output bus line loads \( Q7-Q10 \) do not play a role as a pullup since column selection transistors \( Q12 \) and \( Q14 \) are off in the unselected column. Therefore, the high-impedance pullup results in a large voltage swing in the unselected bit line. The low level of the bit line in this period is lower than that in the column-selected read operation. The low level varies according to the channel width of MOS transistors of the memory cells in the column. The lowest level of the bit line has to be set higher than the largest \( V_{FL} \) of memory cells in the column to retain the data.
4) **Power Dissipation Condition:** In each column dc current flows into the memory cell connected to the selected word line. The power dissipation by the current takes 10—30 percent of the total power dissipation. The power dissipation of the memory cell mainly depends on the size of the access transistors. The pull-up devices Q5—Q10 do not contribute to the power dissipation. As the bit line and input/output bus line are discharged by this current, they determine the access time. In this way the power dissipation is also a limiting factor in the design of the cell.

The optimum sizes of the access transistor and the inverter transistor are determined by the four conditions mentioned above and by the design rules. The range of the transistor dimension for proper read/write operation was obtained from circuit simulations. The result is shown in Fig. 5. In this figure it is also shown that the size mismatch reduces the design margin of the cell. The curves 1)—4) in the figure correspond to the Conditions 1)—4), respectively. The bit line level of the transient write condition was set to \( V_{FL} - 0.75 \) V. The 5 curves show the current that flows into the memory cell.

In this way the transistor size region in which the memory cell operated successfully was obtained. According to the above discussion, the channel widths of the access transistors Q3 and Q4 and bit line load transistors Q5 and Q6 were determined to be 4 and 24 \( \mu \text{m} \) with the fixed inverter transistor size of 8 \( \mu \text{m} \) which was chosen from the limitation of the cell size. The current that flows into the memory cell is about 200 \( \mu \text{A} \) per column. The designed memory cell fabricated by double polysilicon technology is illustrated in Fig. 6. The cell size is 22.8 \( \times \) 27.6 \( \mu \text{m} \).

**IV. Experimental Results**

The designed cell was applied to a 16 kbit static RAM. The circuit block diagram of the RAM is illustrated in Fig. 7. Fig. 8 shows the Schmoo plot of the supply voltage and the substrate bias voltage with the following test patterns.

1) MARCH
2) ROW STRIPE
3) COLUMN STRIPE
4) CHECKER BOARD
5) ADDRESS COMPLIMENT
6) ROW GALLOPING
7) COLUMN GALLOPING.

The figure shows that the dc design described in the previous section could give sufficient dynamic characteristics. Address access time of 40 ns and chip select access time of 40 ns were obtained at \( T = 25^\circ \text{C}, V_{CC} = 5 \) V and \( I_{CC} = 80 \) mA. A minimum write pulse width of 10 ns was obtained.

The power dissipation of the RAM was 400 mW in the active mode and 28 mW in the standby mode. 16 percent of the active power is dissipated at the columns. Only 2 percent of
the active power and 30 percent of the standby power are dissipated at the memory cell array, and the remainder is dissipated in the peripheral circuits. A photomicrograph of the 16 kbit RAM is shown in Fig. 9. The chip size is $4.8 \times 3.7$ mm$^2$. A little more than half of the chip area is devoted to the memory cell array while the rest of the area is utilized by the peripheral circuits and interconnections.

V. CONCLUSION

Using the novel design criteria that deal with the strength of latch, the high-density cell that has a sufficient margin against a mask misalignment is achieved. A 16 kbit static RAM using this memory cell has 40 ns access time at 400 mW power dissipation and has a wide operating margin. These design criteria may be more necessary for static RAM's designed with smaller dimensional MOS transistors.

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REFERENCES


Kenji Anami was born in Oita, Japan, on August 11, 1950. He received the B.S. degree in electronic engineering from Kyushyu University, Fukuoka, Japan, in 1973. He joined the Semiconductor Research and Development Division, Mitsubishi Electric Corporation, Hyogo, Japan, in 1973. From 1973 to 1977 he worked on DSA MOS (DMOS) RAM's and DSA MOS gate arrays. Since 1978 he has been engaged in the design of static MOS RAM's. He is currently involved in the design of 64 kbit CMOS static RAM's.

Mr. Anami is a member of the Institute of Electronics and Communication Engineers of Japan.

Masahiko Yoshimoto was born in Tokushima, Japan, on January 25, 1953. He received the B.S. degree in electronic engineering from Nagoya Institute of Technology, Nagoya, Japan, in 1975, and the M.S. degree in electronic engineering from Nagoya University, Nagoya, Japan, in 1977.

He joined the Mitsubishi Electric Corporation, Tokyo, Japan, in 1977 and is now a staff member of the Mitsubishi LSI Research and Development Laboratory, Hyogo, Japan. Since 1978, he has been engaged in the design of static MOS memories. He is currently involved in the development of VLSI CMOS RAM's.

Mr. Yoshimoto is a member of the Institute of Electronics and Communication Engineers of Japan.

Hirofumi Shinohara was born in Hyogo, Japan, on January 2, 1954. He received the B.S. and M.S. degrees in electrical engineering from Kyoto University, Kyoto, Japan, in 1976 and 1978, respectively.

In 1978 he joined the LSI R&D Laboratory, Mitsubishi Electric Corporation, Itami, Japan. Since then he has been engaged in the development of static MOS RAM's.

Mr. Shinohara is a member of the Institute of Electronics and Communication Engineers of Japan.

Yoshihiro Hirata was born in Osaka, Japan, on September 30, 1953. He received the B.S. and M.S. degrees in science from Kyoto University, Kyoto, Japan, in 1976 and 1978, respectively.

He joined the Mitsubishi Electric Corporation, Tokyo, Japan, in 1978 and is now a staff member of the Semiconductor Division, Hyogo, Japan. He has been engaged in the development of LSI.

Mr. Hirata is a member of the Chemical Society of Japan.

Fig. 9. Photomicrograph of the 16 kbit static RAM. Chip size is $4.8 \times 3.7$ (17.76) mm$^2$.
Approximation of Wiring Delay in MOSFET LSI

TAKAYASU SAKURAI, MEMBER, IEEE

Abstract—Two approximation methods for wiring delay in MOS LSI are studied. One is analytical and the other is a lumped circuit approximation. The basic model for wiring is a distributed CR line with a drive MOSFET at one end and a capacitive load at the other end. Simple approximated formulas for the delay and the step response of this model are obtained.

Approximation of a distributed CR line by lumped R's and C's combination, which is very useful when incorporated in circuit simulation programs, is also investigated. The widely used L ladder circuit model is found to be a poor approximation, while \( \pi \) and T ladder circuit models give satisfactory results. The simplest circuits that approximate the interconnection line within a given tolerant error are tabulated under various drive and load conditions.

LIST OF SYMBOLS

- \( c \) Capacitance of wiring per unit length
- \( r \) Resistance of wiring per unit length
- \( L \) Length of wiring
- \( C \) Total capacitance of wiring (=\( c \cdot L \))
- \( R \) Total resistance of wiring (=\( r \cdot L \))
- \( c_t \) Load capacitance, including MOS transistor gate capacitance to be driven
- \( r_T \) Equivalent resistance of drive MOS transistor
- \( C_T \) = \( c_t / C \)
- \( R_T \) = \( r_t / R \)
- \( x \) The coordinate from driven point to load
- \( t \) Time
- \( t' \) Normalized time (=\( t / CR \))
- \( s \) Laplace transformed variable for \( t \)
- \( s' \) Laplace transformed variable for \( t' \)
- \( a \) = \(-s' \)
- \( v \) Voltage
- \( V \) Laplace transformed voltage
- \( i \) Current
- \( I \) Laplace transformed current
- \( v_{cc} \) Supply voltage
- \( RELM \) Relative error of minimum pole
- subindex \( D \) Distributed \( CT \) line
- subindex \( L \) \( L \) ladder circuit
- subindex \( \pi \) \( \pi \) ladder circuit
- subindex \( T \) \( T \) ladder circuit, except for \( C_T \) and \( R_T \).

I. INTRODUCTION

In MOSFET LSI, a wiring delay becomes an important factor in determining total delay of a system. Particularly, the delay induced by word lines, bit lines, clock lines, and bus
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