A PDM-Based Digital Driving Technique Using Delta-Sigma (ΔΣ) Modulation for QVGA Full-Color AMOLED Display Applications

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Abstract—We propose a digital driving technique using pulse-density modulation (PDM) for an active-matrix organic light-emitting diode (AMOLED) to effectively suppress the false image contour in conventional pulsewidth modulation (PWM) while achieving considerably low operating frequency. A compact first-order digital ΔΣ modulator provides the PDM signal to the panel. A 2.2-inch QVGA AMOLED system using the proposed technique shows no false image contour problem while allowing relaxed minimum gate scan time.

Index Terms—Active-matrix organic light-emitting diode (AMOLED), ΔΣ modulation, digital driving, false image contour, gate scan time, pulse-density modulation (PDM), pulsewidth modulation (PWM).

I. INTRODUCTION

ACTIVE-MATRIX organic light-emitting diode (AMOLED) is one of the most promising contenders for the next-generation display technology because of its high brightness, wide viewing angle, small thickness, fast response time, low power consumption, and compatibility with a flexible substrate [1]. However, several issues have to be addressed for wide deployment. One of the most difficult challenges is the threshold voltage ($V_T$) shift in the pixel thin-film transistor (TFT) [2]. Since the electric current through OLED is $V_T$ dependent, nonuniform $V_T$ and $V_T$ shift due to stress over time directly degrades the graphic quality, and $V_T$ compensation is crucial for high-performance display applications. Several compensation techniques for $V_T$ shift have been proposed for traditional analog driving such as voltage programming and current programming techniques. The voltage programming $V_T$-shift compensation techniques [3]–[5] can achieve compensation with fast data writing. However, it requires a 4-TFT-1-capacitor [3], 5-TFT-2-capacitor [4], or 6-TFT-2-capacitor [5] pixel structure, which increases the panel and driver circuit complexities. The current programming techniques [1], [6]–[8] achieve better image uniformity by detecting the mobility deviation of the driving TFT as well as the $V_T$ shift. However, they require a 4-TFT-1-capacitor [1], [6], [7], or 4-TFT-2-capacitor [8] pixel structure, which increases the panel and driver circuit complexities. They also suffer from a slow pixel writing speed in lower gray levels [1], [6], [7], so the application to large-scale display is limited. To mitigate this problem, a current mirror structure with a large current mirror ratio can be used [8]. However, the large current mirror ratio causes a TFT-mismatch problem degrading the gray-level uniformity. Recently, a $V_T$-compensation technique using a 2-TFT-1-capacitor pixel in analog driving AMOLED was presented [9]. However, it requires OLED supply voltage programming and still shows 14% variation in OLED current even after the $V_T$-shift compensation, which is not sufficient for high-definition applications.

Digital driving has been proposed as an alternative for a solution to the $V_T$-shift issue with simple pixel and driver circuit topologies [10]. Most topics on digital driving for AMOLED are focused on pulsewidth modulation (PWM) because of its simplicity and compatibility with the traditional frame-based refreshing method. However, PWM suffers from the false image contour problem because of the incompatibility with the human visual system. Several approaches have been proposed to alleviate the false contour issue [11]–[19], but all of them significantly increase system complexity, cause gray-level reduction, and suffer from the incompleteness of motion estimation. We propose a non-frame-refreshing digital driving technique using ΔΣ modulation that can alleviate the false image contour issue without increasing system complexity while providing the same or better resolution and a relaxed gate scan time [20].

II. DIGITAL DRIVING

Fig. 1 shows a simple 2-TFT-1-capacitor pixel structure of an AMOLED panel. The brightness of the OLED is dependent on the current through it, so the driving TFT (M2) is used as a current source to control the brightness of the OLED. However, the $V_T$ of the driving TFT varies due to the stress over time [2], and $V_T$ shift in the TFT directly affects the output gray level, making it difficult to achieve a consistent gray-level expression. To resolve the $V_T$-shift issue, several analog driving $V_T$-compensation techniques are reported [1], [3]–[8]. However, these techniques increase the size of pixel circuits and the complexity...
of driving methods. Fig. 2 shows example pixel structures for voltage programming and current programming, which use at least four TFTs and two capacitors. An efficient alternative is digital driving [10]. It effectively compensates for the $V_T$ shift in the driving TFT with a simple 2-TFT-1-capacitor pixel structure. Fig. 3 shows the AMOLED pixel array photograph with a 2-TFT-1-capacitor pixel used in this study. In digital driving, the driving TFT does not operate as a current source, but as a switch. The data line voltage has only low and high states, which correspond to the turn-on and -off states of the driving TFT [10]. During the turn-off state, there is no current flow through the OLED, so the gray level of the OLED is completely dark, providing excellent dark gray levels. On the other hand, during the turn-on state, the driving TFT has the maximum conductance. Due to its large current driving capacity, most of the panel supply voltage (PVDD) is applied to the OLED, so the current is determined by the PVDD value, minimizing the effect of the driving TFT characteristic and, hence, compensating for the $V_T$ shift as well as the mobility variation in the driving TFT. Fig. 4 is the simulation result of the current-versus-voltage relationship of the driving TFT, including TFT variations. It shows that, even in the presence of strong characteristic variations in the driving TFT, the variations in the currents at turn-on and turn-off states are negligible. Therefore, digital driving can compensate the $V_T$ shift with a simple 2-TFT-1-capacitor pixel structure.

Fig. 5 shows block diagrams of typical analog and digital driving AMOLEDs. Digital driving does not require a digital-to-analog converter (DAC) array or an analog buffer array, which tend to be power-intensive. In the analog driving case, a recently developed hybrid 8-bit DAC for flat panel display [21] reported power consumption of 13.3 mW. Instead, digital driving uses a digital modulator array which has been commonly implemented using a PWM technique. Since the modulator array is composed of digital logic gates and shift registers, it consumes much less power than the DAC and analog buffer arrays do. Consequently, digital driving techniques can save power in panel driving circuits. On the other hand, digital driving techniques need to charge and discharge flat panel data lines more frequently than the analog driving techniques do. The frequent charging and discharging causes higher power consumption in panel. The maximum amount of

Fig. 1. Circuit diagram of the basic AMOLED pixel structure.

Fig. 2. Pixel structures of analog driving techniques. (a) Voltage programming. (b) Current programming.

Fig. 3. AMOLED pixel photograph and its schematic diagram.

Fig. 4. Simulated current–voltage relationship of the driving TFT in the face of different process corners.

Fig. 5. Basic structures of analog driving and digital driving. (a) Analog driving. (b) Digital driving.
power consumed in panel charging and discharging is linearly proportional to the number of subfields used in the digital driving techniques. The power consumption in panel charging and discharging for analog driving is

\[ P_{\text{panel, analog}} = \frac{1}{2} C(\Delta V)^2 f \times N_S \times N_D \]  

(1)

where \( C \) is the capacitance of each data line, \( \Delta V \) is the average difference between the consecutive video voltages in a data line, \( f \) is the frame refresh rate, \( N_S \) is the number of scan lines, and \( N_D \) is the number of data lines. In the case of digital driving, the maximum power consumption in panel charging and discharging, assuming the technique has \( N \) subfields, is

\[ P_{\text{panel, digital}} = \frac{1}{2} NCV^2 f \times N_S \times N_D \times \alpha \]  

(2)

where \( V \) is the excitation voltage, and \( \alpha \) is the probability of toggling between on and off during subfield transition.

We ignore the scan-line charging and discharging power for simplicity since each scan line is charged and discharged only once per frame and, hence, demands much less charging and discharging power.

Although it is hard to directly compare (1) and (2) because \( \Delta V \) and \( \alpha \) are video-dependent, assuming \( \alpha = 1 \) (the worst case in terms of power) and \( \Delta V = V/2 \), the panel charging/discharging power of digital driving can be higher than that of traditional analog driving by \( 4N \) times. For example, assuming a QVGA panel (240 scan lines and 320×RGB data lines), a 60-Hz frame rate, 7-V excitation voltage, \( \alpha = 1 \), \( \Delta V = V/2 \), and 6.6-pF data line capacitance [22], \( P_{\text{panel, analog}} \) and \( P_{\text{panel, digital}} \) are 3×186 \( \mu \)W and 3×4×186 \( \mu \)W, respectively. This analysis demonstrates that \( N \) should be minimized to reduce the panel charging/discharging power penalty. Assuming that the 13.3 mW consumed by the DAC array reported in [21] can be saved in digital driving, a digital driving with 3×4×186 \( \mu \)W will balance the power loss and gain in panel and video driver when \( N = 6 \). Another portion of panel power consumption comes from the pixel OLEDs, which consumes \( IP \times PVDD \times N_P \), where \( IP \) is the average OLED current and \( N_P \) is the number of pixels. Typically, this dominates the AMOLED panel power consumption [23], and, consequently, the potential power penalty of digital driving with large \( N \) is negligible.

Although not explored in this study, we note that digital driving is also a strong contender for monolithically integrated driver circuits using TFTs since it can alleviate the inherent manufacturability issues caused by \( V_T \)-variation in mixed and analog circuits such as the DAC and analog buffer.

III. \( \Delta \Sigma \) MODULATION

A. False Image Contour

Although effective \( V_T \) compensation with an area-efficient 2-TFT-1-capacitor pixel and decreased sensitivity to process, voltage, and temperature (PVT) variations makes digital driving attractive, the traditional digital driving technique using PWM suffers from false image contour. In PWM digital driving, each frame is divided into multiple subfields where the duration of each subfield is proportional to its corresponding bit strength. There is a well-defined frame boundary, and each subfield can be placed anywhere in the frame in any predetermined sequence. The basic assumption is that human visual system integrates the output light intensity exactly over the frame time and recognizes the average. The frame refreshing and fixed subfield architecture can result in false image contour when the relative location between the human visual system and the display is not stationary, as shown in Fig. 6. This can happen at certain gray levels when an object on a display moves fast or when watching images on display while walking or driving.

A number of techniques have been proposed to mitigate the false image contour issue in PWM digital driving. The proposed techniques include motion estimation techniques [11], [12], modified subfield distribution [18], [19], optimal subfield distribution [13]–[15], and ramp-wave-controlled PWM [16], [17]. Motion estimation techniques [11], [12] require a complex algorithm to estimate the motion correctly and demand intensive computation for motion estimation processing. Modified subfield distribution techniques [18], [19] use alternating subfield sequences instead of using a fixed binary subfield sequence. These methods add complexity in the driver circuit and suffer from reduced gray scale and motion blur. In optimal subfield distribution techniques, the driver selects the optimal subfield arrangement from a lookup table (LUT) by analyzing the image [13]–[15]. These methods use a complex image analysis algorithm and demand extra time and hardware resources for the analysis. Ramp-wave-controlled PWM techniques effectively eliminate the false contour problem [16], [17] at the expense of a complex pixel structure. The comparator-type pixel circuit in [16] needs a 4-TFT-3-capacitor pixel topology and the clamped inverter-type circuit in [17] uses a 4-TFT-1-capacitor pixel topology, which diminish the advantages of digital driving.

The proposed digital driving technique using \( \Delta \Sigma \) modulation holds all advantages of digital driving and alleviates the false image contour issue without suffering from the drawbacks in the aforementioned PWM-based techniques. Unlike PWM that has no feedback loop, the \( \Delta \Sigma \) modulator uses time-delayed feedback and generates a pulse-density modulated (PDM) signal that has memory. To conceptually show the difference between the two digital driving techniques, we use a simplified timing example with fixed integration duration. Assuming
Modulator Topology

![Example of incorrect integration due to distinct frame boundary](image1)

Fig. 7. Example of PWM waveform which shows false contour condition.

![PDM wave is not affected by the integration window position since it has no clear frame boundary](image2)

Fig. 8. Example of PDM waveform with increasing gray level.

256-gray-levels PWM with a simple binary subfield length allocation, Fig. 7 shows the PWM output waveform for increasing gray levels from 125 to 129. If we integrate the signal over each frame from one frame boundary to the next frame boundary, the output will reconstruct the original gray levels. If the integration windows are not aligned with the frame boundaries, the output will reconstruct wrong gray levels, as shown at the bottom of Fig. 7. The distortion is responsible for the false image contour, which requires a lot of resources for compensation. In the case of the ΔΣ modulator that generates PDM signal, because of its memory property, the previous inputs to the modulator affect current output. Unlike PWM, as long as the pulse density is sufficiently high, the temporal shift of the integration windows does not affect the integrator output as depicted in Fig. 8. Since data of the previous frames affect the current frame pulse density output, it is different from the traditional frame-refreshing techniques. This non-frame-refreshing property makes it unique and effective in suppressing the undesirable false image contour without using any extra techniques. We note that the examples in Figs. 7 and 8 are simplified for clarity, and the actual gray-level transition and integration that can cause false image contour occur much more slowly over much longer time duration.

B. ΔΣ Modulator Topology

A block diagram of the first-order ΔΣ modulator used in this study to generate the PDM signal is shown in Fig. 9. \( X(z) \) is 8-bit digital input, \( E(z) \) is quantization noise, and \( Y(z) \) is PDM 1-bit output stream. The 1-bit quantizer converts incoming input \( X(z) \) into 1-bit PDM output \( Y(z) \), and the quantization error, the difference between \( X(z) \) and \( Y(z) \), is delayed and added to the input using an 8-bit adder, which forms a delayed feedback loop.

The transfer function of the system is

\[
Y(Z) = X(Z) + (1 - Z^{-1})E(Z),
\]

(3)

Equation (3) shows that the quantization error \( E(Z) \) is high-pass filtered. This noise shaping is an inherent property of ΔΣ modulation and is the key for obtaining the target 8-bit gray scale using a coarse temporal resolution compared with that of PWM. The noise shaping can be further improved by using a higher order ΔΣ modulator. Unfortunately, it is not trivial in electro-optic systems like AMOLED. The order of the low-pass filter (LPF) placed after the modulator to average the digital 1-bit stream needs to be one order higher than the order of the ΔΣ modulator to effectively exploit the reduced in-band noise by noise shaping [24].

Once the digital 1-bit stream is converted into an optical signal by pixel OLED, the slow response of human visual system works as a LPF where the system designer has no control. In this work we use a human visual system model based on the work presented in [25], [26]. The photoreceptor in human eyes is equivalent to an adaptation amplifier that is composed of complex combinations of highpass and lowpass filters [25], [26]. There exist two main poles with cut off frequencies 3.18 Hz and 1.59 Hz [25], and for the following analysis and simulations we use two cascaded single-pole LPFs to model the human visual system. Consequently, a first-order ΔΣ modulator is a natural choice because of the proximity of the human visual system to a second-order LPF. The 8-bit input ΔΣ modulator can be implemented using an 8-bit adder [24]. The 8-bit residue is equivalent to the difference between the input and the output of the ΔΣ modulator. The residue can be stored in a register and added to the following input to complete the negative feedback loop. The carry output of the adder represents the pulse-density modulated 1-bit stream. The application of the modulator to a pixel array requires a residue register array, about which is discussed in Section V.

IV. SIMULATION

A. Simulation Models of PDM and PWM Systems

We compare the traditional PWM and the proposed PDM digital driving techniques through simulation to evaluate their performance. Fig. 10 shows the first-order ΔΣ modulation system using an 8-bit adder and an 8-bit residue buffer. The simulated and tested oversampling ratio (OSR), the ratio between the sampling rate of the ΔΣ modulator and the input data rate, ranges from 7 to 17. The minimum pulsewidth of the 1-bit PDM output is \( T_{\text{Frame}}/\text{OSR} \), where \( T_{\text{Frame}} \) is one frame time,
typically 1/60 s. Fig. 11 shows the PWM digital driving system with the binary-weighted pulse generator used in the simulation. For 8-bit input data, the minimum pulselength of the PWM 1-bit output stream needs to be $T_{\text{Frame}}/2^8 - 1 = T_{\text{Frame}}/255$. The simulation uses the second-order LPF model for human visual system described in Section III for both of the digital driving techniques. For simplicity, the simulation considers only one pixel signal.

### B. Ramp Input Analysis and False Contour Suppression

One of the convenient ways to check the false image contour is by using a ramp input analysis. In this simulation, the input sweeps from gray 0 to 255 by one gray step every frame. Fig. 12 shows the output signal spectrums for the two digital driving systems before the LPFs. Fig. 12(a) shows the inherent noise-shaping property of the ΔΣ modulator, and the noise shaping significantly reduces the low-frequency noise floor. Another important observation is that the PDM output spectrum does not have the harmonic tones of the 60-Hz frame frequency which exist in Fig. 12(b). The spectrum demonstrates the unique non-frame-refreshing property of the ΔΣ modulator. Fig. 13 shows the output spectrums after the LPFs. Compared with the PWM output spectrum, the PDM output shows lower noise floor at low frequencies.

The time-domain responses probed at the outputs of the LPFs are plotted in Fig. 14. The PWM output, shown in Fig. 14(a), shows distortions around gray levels 64, 128, and 192, which are responsible for the false image contour. On the contrary, the PDM output curve is distortion free as shown in Fig. 14(b). The time-domain response results demonstrate the effectiveness of the proposed digital driving technique using a ΔΣ modulator in suppressing the false image contour without using any complicated extra circuits. A simulated picture with the false image contours in a PWM system, marked with dotted lines, is also shown in Fig. 15(a). Fig. 15(b) shows an image capture of the 2.2-in QVGA AMOLED panel that uses the proposed ΔΣ modulation digital driving. No false image contour was observed in the typical conditions that result in false image contour such as shaking with a still image and watching fast moving images. The details about the implementation are discussed in Section V.

### C. Resolution and Gate Scan Time

To evaluate the resolutions of the two digital driving systems, the ratio between the fundamental tone power and the distortion tone or noise power is estimated while applying a triangle wave input. A triangle wave is used for simulation simplicity, and the 8-bit input sweeps up and down between levels 0 and 255 with a triangle wave frequency of about a 1-Hz and 60-Hz frame rate. Figs. 16 and 17 show the power spectrums of the
output signals from the PWM and PDM systems, respectively. OSR 13 is used for the PDM. Since triangle waves have only odd harmonics, we estimate the resolution by measuring the ratio between the fundamental tone and the second-order harmonic tone or the noise floor. The ratios for the PWM and PDM spectrums in Figs. 16 and 17 are 50 and 70 dB, respectively, which correspond to 8- and 11.2-bit resolution, respectively. Although the resolution of a display system depends on several factors, and hence the triangular wave simulation alone cannot provide the true resolution, the simulation results show that the proposed digital driving technique using $\Delta\Sigma$ modulator is capable of providing a close or even better resolution compared with PWM digital driving largely due to its noise-shaping property.

The resolution of a $\Delta\Sigma$ modulator depends on the OSR: the higher the OSR, the better the resolution. Fig. 18 shows the estimated resolutions based on the triangle wave simulations for different OSRs. The performance improvement with increasing OSR comes at the cost of processing complexity and the reduction in the minimum pulsewidth of the 1-bit output. Since the data driver needs to write the next bit to each pixel after the minimum pulsewidth duration, the available minimum gate scan time, which is the time allowed for charging or discharging each data line, is inversely proportional to the OSR, as shown in Fig. 18. The gate scan-time estimation depicted in Fig. 18 assumes a QVGA panel ($320 \times 240 \times RGB$). Even with OSR 17, the gate scan time is 12.3 ns, which is much longer than that of the 8-bit input PWM of about 0.85 ns. The longer gate scan time relaxes the requirement on driver operation speed, which is a significant advantage for larger size and higher resolution display panel applications.

### D. Idle Tones

One drawback of $\Delta\Sigma$ modulation is idle tone. When the input gray level stays constant, the PDM output shows periodic tones called idle tones. The idle tones can be described as

$$\text{Idle tones} = n f_S \times \frac{2^0 \times b[0] + \cdots + 2^7 \times b[7]}{255}$$

where $n$ is a positive integer number and $f_S$ is sampling frequency. For example, if the input stays at gray level 6, binary value [0 0 0 0 0 1 1 0], and $f_S$ is 420 Hz, the idle tones resulting from $b[1]$ will appear at 3.29 Hz, 6.59 Hz, 9.88 Hz and so on, and the idle tones resulting from $b[2]$ will appear at 9, 6.59, 13.18 Hz, and so on. Therefore, the low bits of a stationary input provide unwanted idle tones in the low-frequency band. Fig. 19 shows the time-domain output of the $\Delta\Sigma$ modulator when the input gray level is fixed at 6 and the OSR is 7. The idle tone peak to peak is bigger than one gray-level step size. Although the simulation results depicted in Fig. 17 show that OSR 7 is enough for 8-bit resolution, the system must suppress the idle tone peak to peak below one gray-level step size to claim a practical 8-bit resolution. Fig. 20 shows the simulated idle tone peak-to-peak amplitudes with OSR 7 when the input data is fixed at different gray levels. There exist some low, mid and high gray levels, marked with dotted circles in Fig. 20, that show a significant level of idle tones. Those are the gray levels that have several low bits set to high. A similar simulation with OSR 13, depicted in Fig. 21, shows that the idle tone peak to peak can be effectively attenuated by increasing OSR. With OSR 17, the idle tone peak-to-peak amplitudes become less than one gray-level step size at all input gray-level conditions.
E. Flickering

The idle tones associated with low (dark) input gray levels cause another issue. The human visual system tends to be more sensitive to brightness fluctuations at dark gray levels and senses flicker when the fluctuation frequency is less than a critical flicker frequency [27]. Consequently, the idle tones at low gray levels should be reduced further or moved to higher frequencies to prevent flickering. As discussed in the previous section, increasing OSR does both. Fig. 23 shows the output power spectrums with OSR 7 and 13 when the input data is fixed at gray level 6. It shows that increasing OSR shifts the idle tones to higher frequencies and reduces their amplitudes. Another technique for suppressing flicker is dithering. Dithering renders the total error signal, so the output becomes statistically independent of the input signal. In addition, the output signals separated in time become statistically independent of one another, hence dithering weakens the periodicity of the output. A simulation including dithering is conducted using a constant input gray level 6. The dithering is simulated by randomly shifting the input gray levels up and down by one gray level using a random signal generator. The time-domain response, as depicted in Fig. 22, shows that the dithering is effective in reducing the idle tone amplitude. The corresponding power spectrum density shown in Fig. 24 also shows that the dithering reduces the low-frequency idle tones at the cost of a higher noise floor. We note that the increased noise floor represents the weakened periodicity and that the dithering does not require any changes in the $\Delta\Sigma$ modulator design because the input data need to be dithered before entering the modulator.

V. IMPLEMENTATION

The proposed digital driving technique using $\Delta\Sigma$ modulation has been tested using a 2.2-inch QVGA ($320 \times 240 \times$ RGB) AMOLED panel with a 2-TFT-1-capacitor pixel design in poly-Si TFT technology. Fig. 25 shows a block diagram of the implemented test system. A digital video interface (DVI) and transition minimized differential signaling (TMDS) kit delivers the RGB data from the PC to the $\Delta\Sigma$ digital driving AMOLED system. Three $\Delta\Sigma$ modulators for RGB are implemented in an FPGA. As described in Section III, three 8-bit adders comprise the three $\Delta\Sigma$ modulators. Fig. 25 shows only one adder for simplicity. Because the three $\Delta\Sigma$ modulators handle data for whole panel, three register buffer arrays (frame memory) are required. We use SRAM as the frame memory. A frame memory buffer is also inserted between the DVI/TMDS and the $\Delta\Sigma$ modulators to isolate the clock timings between the two. Shift register based scan drivers ($\mu$PD160300) are connected to both data lines and scan lines. The source drivers connected to
data lines get the signals from the output of the ΔΣ modulators. A panel clock timing generator controls the source and scan driver timings.

Fig. 26 shows a photograph of the test system setup. A programmable PLL is used to generate a master clock signal for the system excluding DVI/TMDS. The implemented master clock speed ranges from 32 to 80 MHz, which corresponds to OSR from 7 to 17. The supply voltage was set to 7 V. Fig. 27 shows a still image displayed on the AMOLED panel using the proposed ΔΣ modulation. Typical tests using still and moving images to check false image contour result in no false image contour. Flicker was observed in low gray levels when OSR is 11 or less, and is significantly reduced when OSR is increased to 17.

VI. DISCUSSION

Digital driving, both PWM and PDM, is effective in $V_T$ compensation and provides a simple pixel design. Table I summarizes the pixel structures, gray-level uniformities ($V_T$ compensation), and ease of applications to large-size panels for typical analog $V_T$-compensation techniques [28] and the proposed digital driving technique using ΔΣ modulation. The proposed digital driving technique has advantages of both the analog voltage and current programming techniques. In addition to the advantages of simple $V_T$ compensation and efficient false image contour reduction, which is not trivial in the traditional PWM digital driving, the proposed digital driving using ΔΣ modulation also provides an increased gate scan time. Table II compares analog and digital driving techniques for their gate scan time, number of subfields, power consumption for panel charging and discharging, and power consumption for panel driver. In the table, $T_{Frame}$ is frame period, $N_G$ is the number of gate lines, and $N_S$ is the number of bits of input data. The power consumed by pixel
OLEDs is not included since the power is minimally dependent on driving techniques. Although the proposed $\Delta \Sigma$ modulation technique has a power penalty compared with the PWM digital driving, the penalty is not significant, and the elongated gate scan time of the proposed digital driving technique significantly relaxes the system timing requirement as evidenced by the scan line frequency comparison in Table III.

### VII. CONCLUSION

We present a new PDM digital driving technique for AMOLED using $\Delta \Sigma$ modulation and its application to a 2.2-in QVGA AMOLED panel with a 2-TFT-1-capacitor pixel topology. The proposed technique holds all of the advantages of the traditional PWM digital driving technique such as negligible sensitivity to TFT $V_T$ shift and excellent dark level expression. In addition, the proposed PDM digital driving alleviates the problematic false image contour problem of the traditional PWM digital driving technique without using any complicated circuits, and provides comparable or better image quality with a significant relaxed timing requirement. In-depth time- and frequency-domain analysis techniques have been developed and applied to quantitatively describe the digital driving system performances including resolution, false image contour, idle tones and flickering. The simulation, implementation, and test results demonstrate the effectiveness of the proposed digital driving technique using $\Delta \Sigma$ modulation.

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