Hybrid CORDIC Algorithms

Shaoyun Wang, Vincenzo Piuri, Senior Member, IEEE, and Earl E. Swartzlander, Jr., Fellow, IEEE

Abstract—Each coordinate rotation digital computer iteration selects the rotation direction by analyzing the results of the previous iteration. In this paper, we introduce two arctangent radices and show that about 2/3 of the rotation directions can be derived in parallel without any error. Some architectures exploiting these strategies are proposed.

Index Terms—CORDIC algorithm, elementary function, Givens transformation, planar rotator, CORDIC architecture.

1 INTRODUCTION

The COrordinate Rotation Digital Computer (CORDIC) algorithm is a well-known and widely-studied iterative technique [1], [2] for evaluating many basic arithmetic operations and mathematical functions. It is a bit-recursive algorithm that computes a sequence of vectoring or rotation operations, according to the selected value of the coordinate parameter, in a fixed number of micro-iterations.

The CORDIC vectoring algorithm, usually denoted by \( \text{CORDIC}_v \), is implemented as a sequence of micro-iterations, each of which computes a single coordinate rotation. The resulting output coordinates \((x', y')\) are expressed as:

\[
x' = z + \sin \alpha \cdot z' \\
y' = z - \cos \alpha \cdot z'
\]

where the iterations are performed for \( \forall i, i = 0, 1, 2, \ldots, N - 1 \). The coordinate parameter \( m \) identifies the coordinate system type (namely, circular, linear, and hyperbolic coordinates for \( m \) equal to 1, 0, and \(-1\), respectively). The rotation direction \( \alpha \) for rotation is \( \alpha = -\text{sign}(z) \), while, for vectoring, it is \( \alpha = \text{sign}(x, y) \). For \( m = 1 \), the shift sequence \( S(1, i) \) is defined by \( S(1, i) = 0, 1, 2, 3, 4, 5, \ldots \). The rotation angle \( \alpha_{i,j} \) is given by \( \alpha_{i,j} = \arctan 2^{-S(i,j)} \arctan 2^{-S(i,j)} \).

For each iteration performed, there is a scale factor \( k_{i,j} \) which corrects the amplification introduced by the linearized “rotation” in the \( x \) and \( y \) coordinates. With the above assumptions, \( k_{i,j} = \sqrt{1 + \alpha_{i,j}^2} \).

The functions directly computed by these CORDIC iteration equations, according to the selected value of the coordinate parameter, are summarized in Table 1. With the appropriate initial values of \( x, y, \) and \( z \), we can compute various elementary functions.

TABLE 1

<table>
<thead>
<tr>
<th>Coordinate System</th>
<th>rotation ( y_n \rightarrow 0 )</th>
<th>vectoring ( z_n \rightarrow 0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circular ( m = 1 )</td>
<td>( x_n = \frac{1}{\alpha} (x \cos y - y \sin z) )</td>
<td>( x_n = \frac{\alpha}{1 + \alpha^2} (x^2 + y^2)^{1/2} )</td>
</tr>
<tr>
<td>Linear ( m = 0 )</td>
<td>( y_n = x )</td>
<td>( y_n = x )</td>
</tr>
<tr>
<td>Hyperbolic ( m = -1 )</td>
<td>( y_n = \frac{1}{\alpha} (x \cosh y + y \sinh z) )</td>
<td>( y_n = \frac{\alpha}{1 + \alpha^2} (x^2 - y^2)^{1/2} )</td>
</tr>
</tbody>
</table>

Many papers have been published on the design of advanced CORDIC processors to enhance the performance or to reduce the circuit complexity [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16]. The system latency has been reduced or the throughput has been increased by adopting general digital design techniques [4], [5], [6], [7].

An approach to anticipate the direction of each CORDIC rotation with some possible limited error has also been introduced [5]. The error in the result can be avoided either by appending rotations [8] or by limiting the input range [9]. Null rotations are used to enhance the convergence speed of the algorithm with the side effect of a variable scale factor, depending on the specific sequence of rotations actually applied [10], [11].

In this paper, we analyze the parallelism which is intrinsic in the CORDIC algorithm for the rotation mode only. For simplicity’s sake, we consider only the circular coordinates; similar schemes have been developed also for linear and hyperbolic coordinates [13]. As in many applications requiring function generation, we suppose that the rotation angle is given at run time in the standard binary representation, i.e., it is not the result of a previous vectoring operation. We generalize the approach of [5] by abstracting from a specific architecture and from a single optimization goal. In Section 2, we show that, in a CORDIC processor having significant word size equal to \( N \) (not including the sign bit),...
the rotation directions from iteration \( N = \left\lceil \frac{\log_2 3}{3} \right\rceil \) on can be derived in parallel for the rotation mode without any error. This result is exploited by introducing the hybrid radix sets and the Hybrid CORDIC Algorithms. In Section 3, we derive families of architectures providing alternatives to the designer for a better trade-off analysis between circuit complexity and performance.

2 THE HYBRID CORDIC ALGORITHMS

The essence of the CORDIC algorithm is a representation of an arbitrary angle by using a set of constant angles \( \{a_i\} \) instead of a normal radix. This set is acting like a radix. Therefore, we may choose another set to represent the same angle just like what we do in representing numbers with different radices.

The initial angle \( \theta \) is represented by a set of arctangent constants, called Arc Tangent Radix (ATR) [1]. For the circular coordinates, the radix set is:

\[
\{a_0, a_1, ..., a_{N-1}\} = \{\arctan 2^0, \arctan 2^{-1}, ..., \arctan 2^{-N+1}\},
\]

which satisfies the CORDIC convergence theorem [2]:

\[
a_i - \sum_{j=i+1}^{N-1} a_j < \alpha_{N-1}.
\]

In order to determine the actual value of \( a_i \) for any \( i \), all the previous iterations have to be computed before the evaluation of \( a_i \). This sequential dependence of the radix system induces two bottlenecks in the CORDIC algorithm with respect to parallelization: the generation of the rotation directions and the application of the computed rotations. This second operation cannot be parallelized completely since each rotation must be applied to the vector generated by the previous rotations. Some partial parallelization is possible by merging two conventional CORDIC iterations into the same cycle, but the accuracy is slightly affected [14]; merging cannot be extended to a higher number of conventional CORDIC iterations since the induced error becomes unacceptable. Also, in the low latency architecture in [5], the rotations are applied sequentially after parallel generation of the corresponding group of rotation directions. A completely parallel and error-free generation of the rotation directions is not possible. In fact, the rotation directions are generated in parallel only within the group of the associated CORDIC iterations; but one group can be generated only after the completion of the previous group.

In this paper, we show that the computation of the rotation directions can be partially parallelized without affecting the accuracy by introducing new hybrid radix systems.

The Hybrid Radix Sets

The circular ATR values approach the radix-2 coefficients progressively for increasing values of the CORDIC iteration index. In fact,

\[
\lim_{k \to \infty} \frac{\tan 2^{-k}}{2^{-k}} = 1.
\]

Figs. 1 and 2 compare the circular ATRs and the radix-2 ATRs. After the first few iterations, the error is less than the cube of the radix-2 ATR values. If the iteration index \( i \) is large enough, the error in assuming that radix-2 coefficients are the same as circular ATRs is negligible in the finite precision \( N \)-bit representation. Therefore, if radix-2 is adopted as the radix set for the least significant part of the rotation directions, instead of the circular ATRs, the least significant part of the rotation directions will have about the same precision as the corresponding conventional ATRs.

Based on this remark, we define the Mixed-Hybrid Radix Set:
Mixed-Hybrid Circular ATR =
\[
\{ \arctan 2^{-0}, \arctan 2^{-1}, \ldots, \arctan 2^{-n+1}, 2^{-n}, \ldots, 2^{-N+1} \}
\]
The least significant part is still obtained by approximating the circular ATR by the radix-2. The rotation directions for this part are, as usual, given by \( \sigma = \{-1, 1\} \) being \( i = n, n + 1, \ldots, N - 1 \). Their parallel generation and their application are performed as in the Mixed-Hybrid case. The most significant part is compressed into only one radix to formally describe the single iteration for \( \theta_i \). For \( \sigma_{n-1} \), the definition of rotation direction is extended to represent any possible angle \( \theta_i \) by compressing the circular ATR iterations from the initial one to the \((n-1)\)th one, without modifying \( \theta_L \). Formally, it is:
\[
\sigma_{n-1} = \frac{\theta_H}{\arctan 2^{-n+1}} = \sum_{i=0}^{n-1} \theta_i 2^{-i} / \arctan 2^{-n+1}.
\]
The rotation angle \( \theta_i \) for this preliminary rotation is directly available from \( \theta \). Its application cannot be performed by using (1), since more than one angle value is actually taken into account. The results must be generated—directly and exactly—from the value of \( \theta_i \), e.g., by using such an angle to select \( x_{n-1} \) and \( y_{n-1} \) in a lookup table, including the scale factor.

For both of the Hybrid CORDIC Algorithms, convergence is guaranteed, since they are correct with respect to the condition imposed by (3) for the circular coordinates or similar for the linear case, as stated by Theorem 1.

**Theorem 1.** The Hybrid CORDIC Algorithms satisfy the CORDIC convergence theorem.

**Proof.** In the Hybrid CORDIC Algorithms, the CORDIC convergence theorem is satisfied by the angles \( \alpha_i \) having \( i \geq n \) since they coincide with the conventional linear ATRs.

Consider now the angles having \( i < n \). In the conventional circular CORDIC Algorithm, (3) is:
\[
A = \arctan 2^{-i} - \sum_{j=+1}^{n-1} \arctan 2^{-j} - \sum_{j=n}^{N-1} \arctan 2^{-j} < \arctan 2^{-N+1} = B.
\]
Since \( \arctan 2^{-i} < 2^{-j} \) (for any \( j \geq 0 \)), it is:
\[
\arctan 2^{-i} - \sum_{j=+1}^{n-1} \arctan 2^{-j} - \sum_{j=n}^{N-1} 2^{-j} < A < B < 2^{-N+1}.
\]
The first and the last terms of the inequality are the terms of (3) for the angles of the most significant part in the Mixed-Hybrid CORDIC Algorithm; as a consequence, this algorithm satisfies the CORDIC convergence theorem.

The most significant part of the Partitioned-Hybrid Radix set is a complete and exact rotation by the angle \( \theta_i \) performed in one step: As a consequence, the algorithm converges to the expected angle \( \theta \) if it is able to converge to the angle \( \theta_L = \theta - \theta_H \), i.e., the angle related to the sequence of iterations for \( i \geq n \). Since we have shown above that these iterations satisfy the convergence theorem, the whole Partitioned-Hybrid...
CORDIC Algorithm satisfies the CORDIC convergence theorem.

**Partitioning the Radix Set**

For both of the Hybrid Radix sets, we need to identify the value of \( n \) that preserves full accuracy. Here, we show that they are identical to the corresponding radix-2 coefficients when \( n = \frac{1}{3} N \).

**Lemma 1.** In an \( N \)-bit fixed-point CORDIC processor, the smallest index \( i^* \), which identifies a circular ATR \( \alpha_i \), having the same \( N \)-bit representation as its trigonometric tangent (absolute error \( \leq 2^{-N} \)) is:

\[
i^* = \left\lfloor \frac{N - \log_2 3}{3} \right\rfloor.
\]

**Proof.** Consider the circular ATR \( \alpha_i = \arctan 2^{-i} \). The error \( e_i \), introduced because of assuming such an angle identical to its trigonometric tangent, is:

\[
e_i = 2^{-i} - \alpha_i = 2^{-i} - \arctan 2^{-i}.
\]

By developing the \( \arctan \) function in its Taylor series, we have:

\[
e_i = 2^{-i} - \left(2^{-i} - \frac{1}{3} \left(2^{-i}\right)^3 + \frac{1}{5} \left(2^{-i}\right)^5 - \ldots\right) \]

\[
= \frac{1}{3} \left(2^{-i} - \frac{1}{3} \left(2^{-i}\right)^3 - \frac{1}{5} \left(2^{-i}\right)^5 + \ldots\right).
\]

Obviously, we have,

\[
\frac{1}{3} 2^{-3i} > e_i = \frac{1}{3} 2^{-3i} - \frac{1}{5} 2^{-5i} + \ldots
\]

The smallest number that can be represented by \( N \)-bit fixed-point number is \( 2^{-N+1} \), when the fractional part is composed of \( N - 1 \) bits. Since we are looking for an ATR index \( i \) which is identical to its tangent, the error induced by our approximation is required to be smaller than the smallest angle representable in the processor word. Therefore, we require that:

\[
2^{-3i} > 2^{-N} \quad 3i + \log_2 3 \geq N
\]

By solving with respect to \( i \):

\[
3i + \log_2 3 \geq N
\]

\[
i \geq \frac{N - \log_2 3}{3}
\]

The minimum value \( i^* \) of the index \( i \) that satisfies this relationship is:

\[
i^* = \left\lfloor \frac{N - \log_2 3}{3} \right\rfloor.
\]

**Theorem 2.** In an \( N \)-bit fixed-point CORDIC processor for the circular coordinate system, the rotation directions that cannot be generated in parallel in the Hybrid CORDIC Algorithms without any errors, comparing to the conventional CORDIC algorithm, are the first \( n \) iterations:

\[
n = \left\lfloor \frac{N - \log_2 3}{3} \right\rfloor.
\]

**Proof.** According to Lemma 1, in the conventional CORDIC algorithm for the circular coordinate system, all ATR \( \alpha_i \) having index \( i \) greater or equal to \( \left\lfloor N - \log_2 3 \right\rfloor \) can be replaced by the corresponding linear ATR \( 2^{-i} \) without affecting the accuracy, being identical to the representation in the \( N \)-bit processor word.

The ATRs of the least significant part are now identical to corresponding radices in the linear case. Therefore, we can apply the standard technique for parallel generation of the rotation directions for the ATRs of the least significant part only.

Consider now the CORDIC iterations starting from the initial one \((i = 0)\) to the one identified by the index \( \left\lfloor N - \log_2 3 \right\rfloor - 1 \). Since the ATRs corresponding to these iterations cannot be replaced by the corresponding linear ATR \( 2^{-i} \) without affecting the accuracy, the related \( \left\lfloor N - \log_2 3 \right\rfloor \) rotation directions cannot be generated in parallel.

About \( \frac{1}{3} N \) iterations must be computed in a strictly sequential way, both for the direction generation and the rotation, without affecting accuracy. If a little error is acceptable, we can apply the solutions proposed in [5] and [14] to this first set of iterations. The subsequent rotation directions can be generated in parallel since they coincide with the representation of the residue rotation angle remaining after the first sequential CORDIC iterations.

### 3 Architectures for the Hybrid CORDIC Algorithms

The previous analysis, as well as the extension to the hyperbolic coordinate system [13], can be exploited to design efficient architectures for trigonometric and transcendental function generators. The architectures for these CORDIC algorithms consist of cascading two CORDIC sub-processors: one for each ATR subset. This obviously leads to a higher circuit complexity, but the latency and the throughput may be enhanced.

The architectural approach for the case of the Mixed-Hybrid CORDIC algorithm is given in Fig. 3. The first sub-processor uses the whole rotation angle \( \theta \) and the initial vector coordinates \( x^* \) and \( y^* \) to generate \( z_{mn}, x_m \) and \( y_m \) at the end of the first \( n \) iterations. The rotation directions are generated sequentially, as in the conventional CORDIC algorithm, or predicted in parallel, with an error in the evaluation of the angle [5]. At the end of these iterations, the most significant part of \( z_m \) is zero. The second sub-processor operates starting from \( z_{nm}, x_m \) and \( y_m \) to generate \( x_N \) and \( y_N \) at the end of the remaining \( N - n \) iterations.
A similar architecture can be designed for the case of the Partitioned-Hybrid CORDIC algorithm, as shown in Fig. 4. The first subprocessor operates a rotation of \( \theta_H \) on \( x^* \) and \( y^* \) and generates \( x_n \) and \( y_n \). The second subprocessor receives these intermediate rotated coordinates and applies the rotation \( \theta_L \) to generate the final \( x_N \) and \( y_N \).

Consider the implementation of the first subprocessor working on the most significant part of the ATR set and performing the first \( n \) CORDIC iterations. The simplest approach consists of a ROM for the whole subprocessor, where the most significant part of \( \theta \) is used as an address. This solution is feasible in terms of circuit complexity only for relatively small values of \( n \), as occurs in several applications. The latency of the whole CORDIC processor is reduced to about 67 percent of the latency of a traditional processor performing \( N \) iterations. Alternative solutions can be envisioned for the Mixed-Hybrid CORDIC Algorithm by using a conventional CORDIC processor based on a sequential machine, a combinatoric (possibly pipelined) CORDIC processor, or combined CORDIC processors merging several iterations in a single cycle with possible ROM-based prediction of the rotation directions [15]. This last class of architectures is an intermediate solution between the completely sequential and the purely combinatoric ones: It allows us to save some circuit complexity with respect to the combinatoric case, while achieving higher performance with respect to the sequential machine at a higher circuit complexity. In [13], we reported the detailed evaluation of these structures.

It is not realistic that we put the initial vector \( x_0 \) and \( y_0 \) into ROM when this architecture is used for planar rotations. However, we do have choices of when to do the multiplication. The first choice is to finish the evaluation of the sin and cos functions and do a multiplication, just like what we do with the scale factor. On the other hand, we can do the multiplication of the outputs of the ROM with \( x_0 \) and \( y_0 \) right after we get the ROM output. Either way, the multiplication cannot be eliminated. Of course, if a carry save adder is used, only one full adder delay is added in either case.

Consider now the second subprocessor. The ROM-based approach is never feasible since the ROM is unrealizable. Suitable solutions are variants of the pipelined and combined architectures [13], [15]. No rotation prediction is necessary since directions can be easily obtained by applying a trivial transformation to the angle representation. Pipelined and combined structures degenerate to a purely combinatoric circuit [5] when \( N - n \) CORDIC iterations are performed in a single pipeline stage or clock cycle.

Even if the architectures for the Hybrid CORDIC Algorithms are very similar at a high abstraction level, their actual circuit complexity may be different, in particular, as Processor 1 is concerned. In fact, for example, the ROM realizing this processor in the Partitioned-Hybrid Algorithm must generate only \( x_n \) and \( y_n \), while an additional memory bank is required in the Mixed case, since the residue angle \( z_n \) also needs to be evaluated. On the other hand, the Mixed case allows for a smaller implementation based on a sequential machine, even though the latency is increased and the throughput is reduced. The designer is thus provided with a wide range of alternative approaches so as to achieve an optimum trade-off between performance and circuit complexity for the specific application envisioned.

4 CONCLUSIONS

In this paper, we showed that, in a CORDIC processor for the circular coordinate system in the rotation mode, the rotation directions for approximately 2/3 of the iterations can be derived in parallel without introducing any error. We generalized the approach of [5] by extracting the arithmetic essence and presenting an abstract view of the partitioned CORDIC iterations. We also derived some families of architectures supporting the CORDIC computation at different levels of cost and performance.

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Shaoyun Wang received the BS degree in physics and the MS degree in electronic engineering from Fudan University, Shanghai, People’s Republic of China, in 1982 and 1985, respectively. He is currently a design engineer at Crystal Semiconductor Corporation, Austin, Texas, where he works on audio commercial products. His research interests are in application specific processing, computer arithmetic, CORDIC algorithms, signal processing architectures and implementations, and neural networks. Previously, he was a lecturer in the Electronic Engineering Department at Fudan University, Shanghai, People’s Republic of China, from 1985 to 1991, where he did research on real-time digital signal processing, distributed signal processing, and neural networks. He is pursuing the PhD degree in electrical engineering at the University of Texas at Austin with the support of a Crystal Semiconductor Fellowship.

Vincenzo Piuri obtained the Dring degree in electronic engineering in 1974 and the PhD in computer engineering in 1989, from the Politecnico di Milano, Italy. He was an assistant professor in electrotechnics and computer science at the Politecnico di Milano and director of the Computer Center of the Department of Electronics and Information, Politecnico di Milano. Since 1992, he has been an associate professor in operating systems at the Politecnico di Milano and a consultant to several Italian public administrations for distributed information systems design.

His research interests include distributed and parallel computing systems, application-specific processing architectures, computer arithmetic, fault tolerance, data coding, neural network architectures, theory and applications of neural techniques for identification, prediction, and control of complex dynamic nonlinear systems. The original results of these researches have been published in more than 100 papers in book chapters, international journals, and proceedings of international conferences.

He served as special session organizer or program chair for several international conferences, as well as guest editor for special issues on neural technologies and architectures in the International Journal on System Architectures, the International Journal on Microelectronic Systems Integration, and the International Journal on Computer-Aided Engineering.

He is a senior member of the IEEE, IMACS, INNS, and AEI. He is secretary of the IEEE Computer Society, North Italy Chapter, and secretary of the IEEE Instrumentation and Measurement Society, North Italy Chapter. He is founding co-chair of the Technical Committee on Emergent Technologies of the IEEE Instrumentation and Measurement Society and founding co-chair of the Technical Committee on Fault Tolerance in VLSI Systems. He is member of the IMACS Technical Committee on Neural Networks.

Earl E. Swartzlander, Jr. is a professor of electrical and computer engineering at the University of Texas at Austin, where he holds the Schlumberger Centennial Chair in Engineering. His research interests are in application specific processing, the interaction between computer architecture and VLSI technology, and the history of calculators. He has made significant research contributions in computer arithmetic, VLSI development, and digital signal processor implementation. Previously, he was with TRW Defense and Space Systems from 1975 to 1990, where he held positions ranging from staff engineer to laboratory manager and, most recently, director of Independent Research and Development for the TRW Defense Systems Group.

He is the hardware area editor for ACM Computer Reviews, a subject area editor of the Journal of Systems Architecture, and editor of the Calculators column of the IEEE Annals of the History of Computing. He obtained his doctorate in computer design with the support of a Howard Hughes Doctoral Fellowship. He is a fellow of the IEEE, an inaugural member of the IEEE Computer Society Golden Core, and is a registered professional engineer in Alabama, California, Colorado, and Texas. He has been honored as a Knight of the Imperial Russian Order of Saint John of Jerusalem Ecumenical Foundation (Knights of Malta), an Outstanding Electrical Engineer of Purdue University, a Distinguished Engineering Alumnus of Purdue University, and a Distinguished Engineering Alumnus of the University of Colorado.

REFERENCES
