ABSTRACT
This paper presents the design of a 3.125Gbps CMOS transimpedance amplifier (TIA) with a novel regulated cascode (RGC) preamplifier. The proposed RGC circuit isolates the large input parasitic capacitance and then improves the bandwidth limitation. This TIA was fabricated in 1P6M 0.18um CMOS process and consumes 11.43mA from 1.8V supply voltage. The TIA achieves a gain of 72dBΩ and 2.4GHz bandwidth when connected to a 0.5pF photodiode.

I. INTRODUCTION
Recently, the demand for higher data rates in wireline and wireless communication systems has greatly increased. As considering such demands, data transmission over optical fiber links is an attractive solution because of wide bandwidth, low EMI, and low channel loss.

In the optical communication system, the front-end transimpedance amplifier (TIA) is a critical building block affecting the whole optical system performance. The most important specifications of the TIA are input noise current, bandwidth, transimpedance gain and power. However, these parameters usually conflict each other and show trade-off characteristics. A number of CMOS TIA’s architectures to mandate careful optimization of the parameters have been reported [1]-[5]. Among these circuit architectures, it is well known that a regulated cascode (RGC) circuit is very popular configuration achieving wide bandwidth, high gain, and low power consumption [3]. Especially, this has an important feature such as being improved the noise current density toward lowering the input impedance associated with the bandwidth [4].

Nevertheless, conventional RGC configuration needs to be more modified to relax the input parasitic effects affecting the bandwidth for gigabit class links. To achieve its low impedance and better isolation, a new RGC TIA based on the conventional RGC topology is proposed in this work, which is especially realized in a 0.18um CMOS technology for targeting 3.125-Gb/s Gigabit Ethernet applications.

This paper is organized as following. Section II discusses some considerations for wide bandwidth design and presents a proposed RGC input stage. The whole TIA block with the proposed architecture and the experimental results are described in Section III. Section IV. Finally, section V concludes the proposed TIA design for 3.125Gbps.

II. CIRCUIT DESIGN
A. Design Considerations for Input Capacitance
Fig. 1 shows the circuitry of a conventional RGC preamplifier with a photodiode. The photodiode converts the incoming optical power to a photocurrent and then it is amplified to be a voltage by the $M_1$ and $R_D$ of RGC preamplifier. The $M_B$ and $R_B$
stage operates as a biasing of M1 and local feedback stage, which reduces the input impedance by amount of its own voltage gain as \((1+g_{mb}R_b)\).

In this circuit, however, the input parasitic capacitor components including photodiode capacitance (\(C_{PD}\)), ESD protection diode capacitance (\(C_{ESD}\)), bonding pad parasitic capacitance (\(C_{PAD}\)), and input parasitic capacitance (\(C_{in,RGC}\)) of RGC circuit itself has very large value compare to other nodes of TIA circuit. It would affect to deteriorate the noise performance as well as 3dB bandwidth. The impacts of bandwidth and noise over the input parasitic capacitor components are approximately described by (1), (2) respectively. It is noted that 3dB bandwidth decreases and input noise current increases as input parasitic capacitance increases.

\[
f_{3db, input} \approx \frac{g_{mb}(1+g_{mb}R_b)}{2\pi(C_{PD}+C_{ESD+PAD}+C_{in,RGC})}
\]

\[
t_e \approx 4kT(G_{ds,B}+1/R_b)
\]

where \(k\) is Boltzmann’s constant, \(T\) is the absolute temperature, \(\Gamma\) is the noise factor of the MOSFET, \(g_{ds,B}\) is the zero-bias drain conductance.

Especially, \(C_{PD}\) as the predominant component has the values of 0.25\(\mu\)F to 1.5\(\mu\)F. In order to meet the >2.4GHz bandwidth requirement for 3.125Gb/s data rate, the input parasitic capacitance must be less than 0.6\(\mu\)F as the input resistance of the RGC circuit is designed at about 100\(\Omega\). Hence, the photodiode capacitance should be at least less than 0.4\(\mu\)F as considering the values of other input’s parasitic capacitor components. It makes selecting various photodiodes with excellent characteristics to limit.

Consequently, the gain of the local feedback stage should be more increased to decrease the input resistance. It finally achieves wide bandwidth and low noise current. However, increasing the gain of the circuit itself could deteriorate the stability and linearity performances of the circuit. Thus, it is needed to develop new circuit methodologies with keeping the advantages of RGC circuit.

### B. Proposed RGC Input Stage to Enhance \(g_{mb}\)

Fig. 2 shows the schematic diagram of a proposed novel RGC preamplifier. The modification is that a positive amplifier consisted of \(M_B1, R_B2\) and \(M_{p1}\) has been inserted into a conventional RGC preamplifier, which provides a better transconductance, \(g_{mbFB}\) as local feedback’s gain. To increase easily the gain without large power consumption, the positive amplifier is cascaded with the negative local feedback amplifier, where \(M_{p1}\) returns the feedback signal to the input of the circuit and then makes the input node to be more virtual-ground.

Now the proposed circuit still more operates as a current buffer. Also, it plays an important role in isolating the large input capacitance since the input impedance is small enough. In addition, since the simple topology of the positive amplifier has small voltage headroom, it doesn’t limit the low voltage operation, linearity and stability of the proposed RGC circuit.

Using the small-signal equivalent model, the input resistance is approximately given by

\[
Z_m(0) \approx \frac{1}{g_{m,M1}(1-A_1) + g_{m,M2}A_2}
\]

where \((1-A_1)\) represents the feedback gain of the local feedback stage of a conventional RGC circuit, that is, \((1+g_{m,B1}R_{B1})\) and the \(A_2\) represents the gain of the cascade local feedback stage of the proposed circuit, \(g_{m,B1}g_{m,B2}R_{B1}R_{B2}\). Note that the equation of (3) means that the input impedance consists of two conductance components in parallel, which formed by two feedback paths. It is clearly seen that the input impedance would be smaller by adding \(g_{m,M2}A_2\) that of the conventional one. Therefore, to maximize this effect, if the second term of \(g_{m,M2}A_2\) is increased, the dominant pole made by large input capacitance would be shifted up a higher frequency.
However, the cascade local feedback path additionally connected to the input port through \( M_{p1} \), can lead to high input noise current density. So, to minimize the noise contribution by \( M_{p1} \), (W/L) of \( M_{p1} \) should be carefully decreased along with operating bias conditions. It is also good choice for reducing input parasitic capacitance, simultaneously. Although \( g_{m, MP1} \) is attenuated, the cascade feedback gain would be compensated for the low input impedance as \( A_2 \) increases more. In simulation results, the bandwidth is extended by about 16.2\% (5.52GHz) at 0.5pF \( C_{PD} \) than 4.75GHz in the conventional one with the same noise current.

**III. TIA DESIGN FOR 3.125Gbps**

The TIA block diagram with the proposed RGC architecture is shown in Fig. 3. It consists of the RGC preamplifier, a single to differential amplifier (S2D), four voltage amplifiers and an output buffer. The front-end preamplifier operates as a transimpedance amplifier. After the current to voltage conversion of this preamplifier, S2D converts the signal to differential pair for better common-mode noise rejecting and widening linear signal swing. A RC-LPF between the TIA preamplifier and one of S2D inputs is used to avoid DC wander and serious high frequency pattern jitter, which has the low cut-off frequency of several kHz. Four voltage amplifiers follow to further increase the signal swing and remove inter-symbol interference (ISI). Which also having a function of equalizer use capacitive degeneration technique to provide additional zero and then generate boosting at high frequencies. In addition, feedback resistors (\( R_f \)) are inserted in there because each poles of voltage amplifiers may be close enough to generate a peaking, which stabilize the circuit stability and also expend the bandwidth. To perform DC-offset cancellation, output buffer and amplifier A1 compose the offset cancellation circuit chain. The cutoff frequency for the offset cancellation is designed to be low enough to avoid baseline wander; with a nominal value of 50 kHz. Also, the output buffer consists of two DC balanced cross-coupled gain stages with a \( f_t \) doubler and source-degeneration load technique to minimize the mismatch, bandwidth reduction and power consumption. It consumes alone 8.85mA, which occupies 77.4\% of the one of the TIA block.

![Chip Microphotograph of a designed 3.125Gb/s TIA](image-url)
IV. MEASUREMENT RESULTS

In Fig. 4, the chip microphotograph of the designed TIA for 3.125Gbps is shown, which is fabricated using a 1P6M 0.18um CMOS technology. The core has an area of 340 x 510um². ESD protection diodes with 150fF parasitic capacitance are included in all pads. The designed IC is directly bonded to the PCB, on there an equivalent circuit of photodiode mounted for EUT measurement.

![Image](image1)

**Figure 5: Measured frequency responses**

Fig. 5 shows the measured transimpedance gain of 72dB and 3dB BW of 2.4GHz with less than 1.2dB in-band ripple for 0.5pF Cpd. Fig. 6 shows the measured group delay. Fig. 7 shows the measured eye diagrams at different data rates of 1.25Gb/s, 2.5Gb/s, 3.125Gb/s and 5Gb/s for 2³¹-1 PRBS. The average input noise current density is 18.12pA/√Hz after de-convolving as shown in Fig. 8. The TIA is consumes 11.43mA at 1.8V power supply. Finally, the measured performance results are summarized in Table 1.

![Image](image2)

**Figure 6: Measured group delay**

**Figure 7: Measured eye-diagrams for 2³¹-1 PRBS**

**Figure 8: Measured output noise of TIA (single-ended)**

IV. CONCLUSION

A low input impedance RGC TIA is designed and implemented in a 0.18-μm CMOS technology. With advantages of the nominal RGC topology, a new proposed RGC architecture relax the large input parasitic effect and then improves the bandwidth limitation made by input components. The designed circuit is suitable for 3.125Gbps optical communication as well as low voltage, low noise operation.

ACKNOWLEDGEMENT

This research was funded by the MSIP (Ministry of Science, ICT & Future Planning), Korea in the ICT R&D Program 2013.
### Table 1: Summary of Performances

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<td>110 (TIA=60, LA=50)</td>
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<td>2</td>
<td>2.1</td>
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<td>(1&lt;1.2dB in-band ripple)</td>
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* FoM= ZT[dB]*X3dB[GHz]/PDC[mW]

### REFERENCES


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